Service Manual

Model #: VIZIO P50HDM

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-TOP Confidential -

Table of Contents

CONTENTS PAGE

Sections

1. Features 1-1

2. Specifications 2-1

3. On Screen Display 3-1

4. Factory Preset Timings 4-1

5. Pin Assignment 5-1

6. BLOCK DIAGRAM 6-1

7. Main Board I/O Connections 7-1

8. Theory of Circuit Operation 8-1

9. Waveforms 9-1

10. Trouble Shooting 10-1

11. Spare Parts List 11-1

12. Complete Parts List 12-1

Appendix

1. Main Board Circuit Diagram

2. Main Board PCB Layout

3. Assembly Explosion Drawing

Block Diagram

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FCC INFORMATION
This equipment has been tested and found to comply with the limits of a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that the interference will not occur in a particular installation. If this equipment does cause unacceptable interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures -- reorient or relocate the receiving antenna; increase the separation between equipment and receiver; or connect the into an outlet on a circuit different from that to which the receiver is connected.

FCC WARNING
To assure continued FCC compliance, the user must use a grounded power supply cord and the provided shielded video interface cable with bonded ferrite cores. Also, any unauthorized changes or modifications to Amtrak products will void the user's authority to operate this device. Thus VINC Will not be held responsible for the product and its safety.

CE CERTIFICATION
This device complies with the requirements of the EEC directive 89/336/EEC with regard to "Electromagnetic compatibility."

SAFETY CAUTION
Use a power cable that is properly grounded. Always use the AC cords as follows – USA (UL); Canada (CSA); Germany (VDE); Switzerland (SEV); Britain (BASEC/BS); Japan (Electric Appliance Control Act); or an AC cord that meets the local safety standards.

Chapter 1 Features

- Wall-mountable
- New WIDE HD Plasma Panel:1366 x 768 (H x V)
- TruSurround XT sound system and DCDi by Faroujia video image
- High definition digital interface – HDMI
- HDCP supportive
- Multiple-screen display (picture-on-picture/picture-in-picture)
- Selectable picture mode
- 4-language On Screen Display
- 2 S-video and Composite video inputs
- 2 Component video inputs
- 2 HDMI inputs
- 6 audio stereos, 1 PC Mini-Jack
- Supporting DVI converted to HDMI
- Closed caption
- Gloss front bezel
- The thinnest model of this size: 99 mm

Chapter 2 Specification

1. OPTICAL CHARACTERISTICS

Item	Specification
Display Pixels	1366 (H) x 768 (V) pixels
Pixel Pitch	0.810 mm (H) X 0.810mm (V)
Pixel Type	Non-stripe
Color Depth	1,024 (R) x 1,024 (G) x 1,024 (B) colors
Active Display Area	1106.5 mm (H) x 622.1 mm(V)
Brightness (panel spec)	1000 cd/m2 (Typical)
(w/glass filter)	Min.300 cd/m
Contrast ratio (panel spec)	8000:1 (Typical, dark room)
Color Coordinates (typical)	
White (Panel spec)	x=0.300±0.02, y=0.300±0.02
White (w/glass filter)	Warm (5400K)
	Standard (6500K)
	Cool (9300K):

2. INPUT SOURCE

RGB Signal： H: support to 30-80KHz
V: support to 60-85Hz
Pixel Clock: support to 108MHz

HDMI Signal： H: 15.734KHz V: 60Hz (480i)
H: 31KHz V: 60Hz (480p)
H: 45KHz V: 60Hz (720p)
H: 33KHz V: 60Hz (1080i)

S-Video： Video (Y): Analog 0.1Vp-p/75Ω
Video (C): Analog 0.286p-p/75Ω

Composite Video signal: H: 15.734KHz V: 60Hz (NTSC)

Component signal: YPbPr/YCbCr

H: 15.734KHz V: 60Hz (NTSC-480i)

H: 31KHz V: 60Hz(NTSC-480p)

H: 45KHz V: 60Hz(NTSC-720p)

H: 33KHz V: 60Hz(NTSC-1080i)

3. INPUT CONNECTORS

Input Label	Connector Type	Input Label	Connector Type
SERVICE	RJ-11 x 1	ANALOG HD1	YPb/Cb Pr/Cr RCA Jack x 3 Audio RCA Jack x 2
DIGITAL HD1	19 pin HDMI x 1 Audio RCA Jack x 2	ANALOG HD2	YPb/Cb Pr/Cr RCA Jackx 3 Audio RCA Jack x 2
DIGITAL HD2	19 pin HDMI x 1 Audio RCA Jack x 2	AV1	RCA Jack (CVBS) x 3 S-video 4 pin mini DIN x 1
RGB	D-sub 15 pin x 1 Mini Jack x 1 (Audio input)	AV2	RCA Jack (CVBS) x 3 S-video 4 pin mini DIN x 1

4. OUTPUT CONNECTORS

a. Audio RCA Jack x 2

b. 3.5mm Mini-jack earphone x 1

5. POWER SUPPLY

Consumption: 550W MAXPower OFF: less than 3W

6. SPEAKER

Output 8Ω/10W (max) X2

7. ENVIRONMENT

Operating

a. Temperature: 0~40℃
b. Relative humidity: 20%~80% RH
c. Altitude: 0~6,560 ft

Non-operating

a. Temperature: -20~60℃
b. Relative humidity: 10%~90% RH
c. Altitude: 0~9,840 ft

8. DIMENSIONS

a. Height: 871 mm
b. Width: 1241mm
c. Depth: 310 mm (with standard), 99 mm (without standard)

9. WEIGHT

a. Net: 55.2 +/- 0.5 kgs
b. Gross: 65.2 +/- 0.5 kgs

Chapter 3 On Screen Display

Main unit button

POWER

MENU

▲

▼

VOL-/◀

VOL+/▶

INPUT

OSD Adjustment

Mode				
Image Settings				
VIDEO	Picture Mode(User, Vivid, Movie, Game, Sport)			
	Brightness(0~100)			
	Contrast(0~100)			
VIDEO	Saturation(0~100)			
VIDEO	Hue(-50~50)			
VIDEO	Sharpness(0~24)			
	Advanced			
VIDEO		Noise Reduction		
VIDEO			Motion(0~16)	
VIDEO			Digital(0~64)	
VIDEO		Fleshtone	Off, High, Moderate, Low	
VIDEO		Dynamic Contrast (0, 1, 2, 3)		
PC		Auto Adjustment		
PC		Image Position		
PC		Phase		
PC		Clocks / Line		
PC		Color Temp		
PC			Warm(5400K)	

PC			Standard(6500K)	
PC			Cool(9300K)	
PC			User	
PC				Red(0~100)
PC				Green(0~100)
PC				Blue(0~100)
Display Settings				
VIDEO	Aspect Ratio	Wide, Normal, Zoom, Panoramic*		
PC	Aspect Ratio	Wide, Normal		
	PIP			
		PIP Mode	Off, Large PIP, Small PIP, POP	
		PIP Position	Top-Left, Top-Right, Bottom-Left, Bottom-Right	
		PIP Input**		
Audio Settings				
	Bass(0~20)			
	Treble(0~20)			
	Balance(-10~10)			
	SRS TS XT(Off, On)			
	Auto Volume(On, Off)			
	Speakers(On, Off)			
	Audio Out***	Fixed Volume, Variable Volume		
Parental Controls				
VIDEO	Password			
VIDEO		Settings		
VIDEO			TV Rating	

VIDEO				TV Youth (Unblocked, Blocked)
VIDEO				TV Youth 7 (Unblocked, Blocked)
VIDEO				TV G (Unblocked, Blocked)
VIDEO				TV PG (Unblocked, Blocked)
VIDEO				TV 14 (Unblocked, Blocked)
VIDEO				TV MA (Unblocked, Blocked)
VIDEO				Unblocked
VIDEO			Movie Rating	
VIDEO				Movie G (Unblocked, Blocked)
VIDEO				Movie PG (Unblocked, Blocked)
VIDEO				Movie PG-13 (Unblocked, Blocked)
VIDEO				Movie R (Unblocked, Blocked)
VIDEO				Movie NC-17 (Unblocked, Blocked)
VIDEO				Movie X (Unblocked, Blocked)
VIDEO				Unblocked
			Block Unrated (No, Yes)	

VIDEO		Change Password		
VIDEO			Please enter new password	
VIDEO			Please re-enter new password	
VIDEO		Clear All (No, Yes)		
Setup				
	Closed Caption			
		Display	Off, CC1, CC2, CC3, CC4, TEXT1, TEXT2, TEXT3, TEXT4	
		Captions on mute (On, Off)		
	Language	English, Français, Español, Italiano		
	Factory Reset (Yes, No)			
	Image Cleaner			
	Firmware Version			

* HDMI and Component 720P/1080i inputs do not support Panoramic.

** See below for detailed information regarding the PiP sources.

Main \ Sub	AV1 (S-VIDEO)	AV2 (S-VIDEO)	AV1 (VIDEO)	AV2 (VIDEO)	Analog HD1	Analog HD2	Digital HD1	Digital HD2	RGB
AV1 (S-VIDEO)		x	x	x	x	x	x	x	x
AV2 (S-VIDEO)	x		x	x	x	x	x	x	x
AV1 (VIDEO)	x	x		x	x	x	x	x	x
AV2 (VIDEO)	x	x	x		x	x	x	x	x
Analog HD1	x		x			x	x	x	x
Analog HD2	x		x		x		x	x	x
Digital HD1	x		x		x	x		x	x
Digital HD2	x		x		x	x	x		x
RGB	x		x		x	x	x	x	

Remark：

(1)：“x” – Indicates which inputs are available for PIP and POP modes.

(2)：For AV1 and AV2, S-Video has priority. If a signal is connected to AV1 S-Video by itself or signals are connected to AV1 S-Video and AV1 Video simultaneously, then S-Video will be the only choice for AV1. If a signal is connected to AV1 Video only, then Video will be the only choice for AV1. The same input priority scheme applies to AV2.

*** When Speakers off

Chapter 4 Factory preset timings

This timing chart is already preset for this plasma monitor.

1. PC analog preset modes

Mode No.	Resolution	Refresh Rate (Hz)	Horizontal Frequency (KHz)	Vertical Frequency (Hz)	Horizontal Sync Polarity (TTL)	Vertical Sync Polarity (TTL)	Pixel Rate (MHz)	Remark
1	640x480	60	31.5	59.94	N	N	25.175	Windows
2	640x480	75	37.5	75.00	N	N	31.500	Windows
3	800x600	60	37.9	60.317	P	P	40.000	Windows
4	800x600	75	46.9	75	P	P	49.500	Windows
5	800x600	85	53.7	85.06	P	P	56.250	Windows
6	⦿1024x768	60	48.4	60.01	N	N	65.000	Windows
7	1024x768	70	56.5	70.07	N	N	75.000	Windows
8	1024x768	75	60.0	75.03	P	P	78.750	Windows
9	1366X768	60	47.7	60.00	P	N	85.500	Windows
10	1280X1024	60	63.98	60.02	P	P	108.000	Windows

Remark： P：positive，N： negative ⦿1024x768 @60 Hz: Primary

2. HD video digital preset modes at HDMI

Mode No.	Resolution
1	480i
2	480p
3	720p
4	1080i

3. HD digital preset modes at DVI

Through HDMI interface by an optional interface cable 2.3.3.1 video input.

3. 1 Video input

Mode No.	Resolution
1	480i
2	480p
3	720p
4	1080i

3.2 PC input

Mode No.	Resolution	Refresh Rate (Hz)	Horizontal Frequency (KHz)	Vertical Frequency (Hz)	Horizontal Sync Polarity (TTL)	Vertical Sync Polarity (TTL)	Pixel Rate (MHz)	Remark
1	640x480	60	31.5	59.94	N	N	25.175	Windows

Chapter 5 Pin Assignment

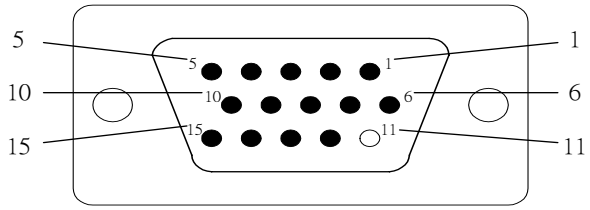
1.Input

There are analog and digital connectors as video input source in this model.

1.1 Analog

1.1.1 RGB Connector

a. Type:	Analog	
b. Frequency:	H: 30-80KHz	V: 60-85Hz
c. Signal level:	0.7Vp-p	
d. Impedance:	75Ω	
e. Synchronization	H/V separate sync:	TTL
	H/V composite sync: Sync on Green	TTL
f. Video bandwidth:	135MHz	
g. Connector type:	15-pin D-Sub, female	

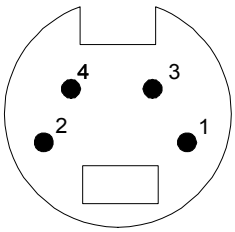


Pin Number	Pin Assignment	Pin Number	Pin Assignment
1	Red video input	9	+5V
2	Green video input	10	Ground
3	Blue video input	11	No connection
4	Ground	12	(SDA)
5	Ground	13	Horizontal sync (Composite sync)
6	Red video ground	14	Vertical sync
7	Green video ground	15	(SCL)

1.1.2 RCA-type (Yellow) Composite Video Connector

a. Frequency:	H: 15.734KHz	V: 60Hz	(NTSC)
b. Signal level:	1Vp-p	Sync (H+V):	0.3V below Video (Y+C)
c. Impedance:	75Ω		
d. Connector type:	RCA jack		

1.1.3 S-Video Connector



1, 2 = GND
3 = Luminance (Y)
4 = Chrominance(C)

a. Frequency:	H: 15.734KHz	V: 60Hz	(NTSC)
b. Signal level:	Y: 1Vp-p	C: 0.286Vp-p	
c. Impedance:	75Ω		
d. Connector type:	4-pin mini DIN		

1.1.4 Y-Cb/Pb-Cr/Pr Component video signal

a. Frequency:	H: 15.734KHz	V: 60Hz	(NTSC-480i)
	H: 31KHz	V: 60Hz	(NTSC-480p)
	H: 45KHz	V: 60Hz	(NTSC-720p)
	H: 33KHz	V: 60Hz	(NTSC-1080i)
b. Signal level:	Y: 1Vp-p	Pb: ±0.350Vp-p	Pr: ±0.350Vp-p
c. Impedance:	75Ω		
d. Connector type:	RCA jack		

1.1.5 PC audio in

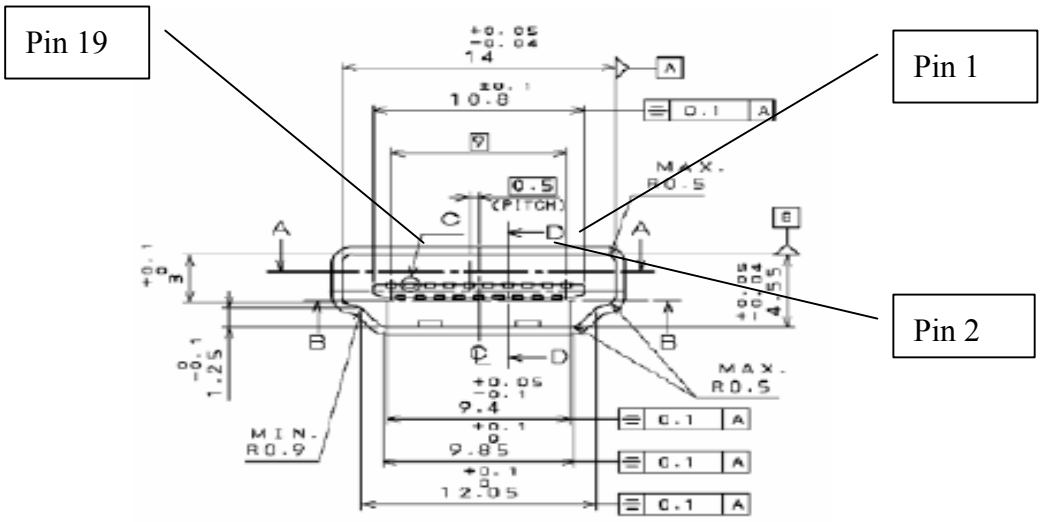
a. Signal level:	1Vrms
b. Impedance:	47KΩ
c. Connector type:	3.5 ϕ mini jack

1.1.6 Video audio in

a. Signal level:	0.7Vrms
b. Impedance:	47KΩ
c. Frequency Response:	250Hz-20KHz
d. Connector type:	RCA L/R:

1.2 Digital - HDMI

a. Frequency:	H: 15.734KHz	V: 60Hz
	H: 31KHz	V: 60Hz
	H: 45KHz	V: 60Hz
	H: 33KHz	V: 60Hz
b. Polarity:	Positive or Negative	
c. Type:	Type A	
d. Pin Assignment:	Please see below	



Pin	Signal Assignment	Pin	Signal Assignment
1	TMDS Data2+	2	TMDS Data2 Shield
3	TMDS Data2-	4	TMDS Data1+
5	TMDS Data1 Shield	6	TMDS Data1-
7	TMDS Data0+	8	TMDS Data0 Shield
9	TMDS Data0-	10	TMDS Clock+
11	TMDS Clock Shield	12	TMDS Clock-
13	CEC	14	Reserved (N.C. on device)
15	SCL	16	SDA
17	DDC/CEC Ground	18	+5V Power
19	Hot Plug Detect		

2. Output

2.1 Earphone

a. Signal level: 1Vrms (max.)

b. Impedance: 32Ω

c. Output: 50 mW

d. Connector type: Earphone mini jack

2.2 Audio output

a. Signal level: 0.7Vrms

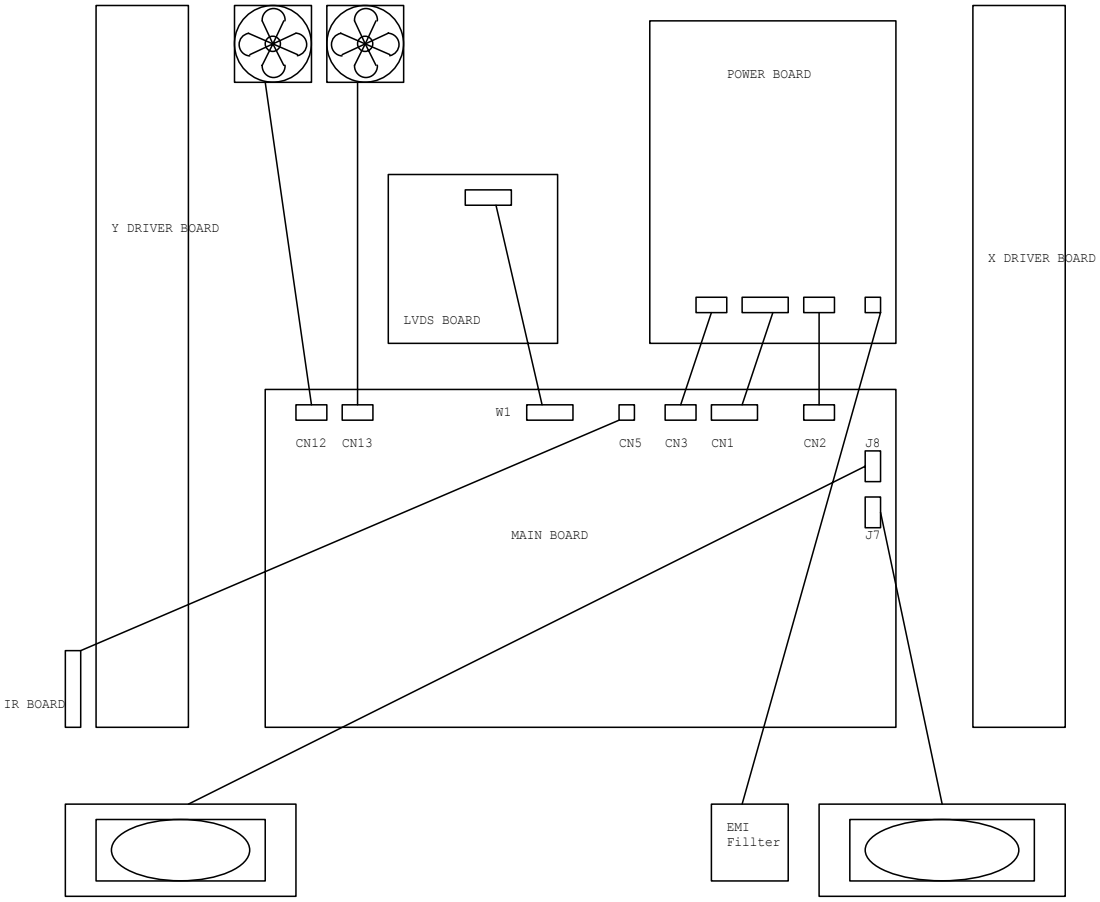
b. Impedance: 47KΩ

c. Frequency Response: 250Hz-20KHz

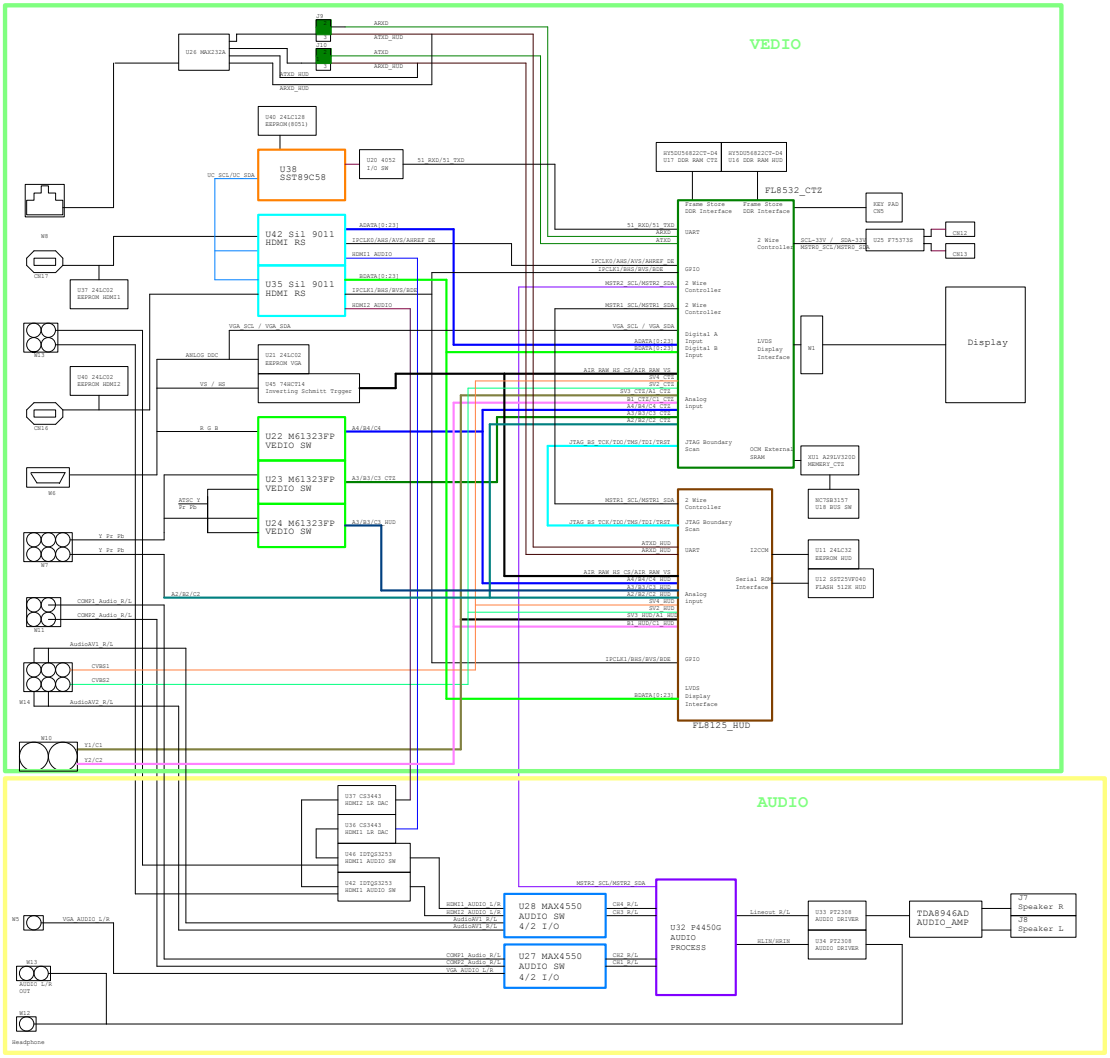
d. Connector type: RCA L/R:

Chapter 6 Block Diagram

System Block Diagram



Main board System Block Diagram



Chapter 7 Main Board Internal I/O Connections

CN1 “DC POWER INPUT’

PIN	Description
1	PDP_+5Vsc
2	PDP_+5Vsc
3	PDP_+5Vsc
4	GND
5	GND
6	GND
7	PDP_+12V
8	PDP_+12V
9	GND
10	GND
11	PDP_+12V_FAN
12	PDP_FGND

CN2 “DC POWER INPUT’

PIN	Description
1	PDP_Audio
2	PDP_Audio
3	GND
4	GND

CN3 “DC POWER INPUT/OUTPUT’

PIN	Description
1	GND
2	VS_ON
3	RLY_ON
4	PDP_+5Vsb

CN5 CONNECTION “KEYPAD”

PIN	Description
1	LED2_KEYPAD
2	KEY_VCC
3	IR
4	ADC_IN2
5	NC
6	GND
7	+3.3V_LBADC
8	ADC_IN1
9	LED1_KEYPAD_BUF
10	GND
P1	GND
P2	GND

CN6 CONNECTION “HDMI/ATSC_UP”

PIN	Description
1	+5V
2	51_TXD
3	51_RXD
4	GND

CN7 CONNECTTION “ODC2BI”

PIN	Description
1	VGA_SCL_CTZ
2	VGA_SDA_CTZ
3	GND

CN12 FAN CONNECTION

PIN	Description
1	NC
2	FANIN1
3	+12V_FAN
4	FGND

CN13 FAN CONNECTION

PIN	Description
1	FANIN1
2	+12V_FAN
3	FGND

J7 CONNECTION “SPEAKER R”

PIN	Description
1	RL-
2	RL+
3	NC

J8 CONNECTION “SPEAKER L”

PIN	Description
1	LL-
2	LL+

W1 CONNECTION “LVDS”

PIN	Description	PIN	Description
1	GND	2	TXA3+
3	TXA3-	4	TXAC+
5	TXAC-	6	GND
7	TXA2+	8	TXA2-
9	TXA1+	10	TXA1-
11	TXA0+	12	TXA0-
13	GND	14	GND
15	+5V_SW	16	+5V_SW
17	+5V_SW	18	GND
19	GND	20	NC
21	NC	22	NC
23	NC	24	TXB3+
25	TXB3-	26	GND
27	VS_ON	28	SCL_33V
29	SDA_33V	30	NC
31	GND		

J3 SELECT KEY POWER

PIN	Description	Default
1-2	+3.3V_I/O	ON
2-3	+5V	OFF

“ON” ADD JUMPER , “OFF” NO JUMPER

J9 CONNECTION “PROGRAMUPDATA”

PIN	Description	Default
1-2	ARXD	ON
2-3	ARXD_HUD	OFF

“ON” ADD JUMPER , “OFF” NO JUMPER

J10 CONNECTION “PROGRAMUPDATA”

PIN	Description	Default
1-2	ATXD	ON
2-3	ATXD_HUD	OFF

“ON” ADD JUMPER , “OFF” NO JUMPER

Chapter 8 Theory of Circuit Operation

The operation of User Interface

The following diagram provides a brief overview of the user-interactive components of the firmware.

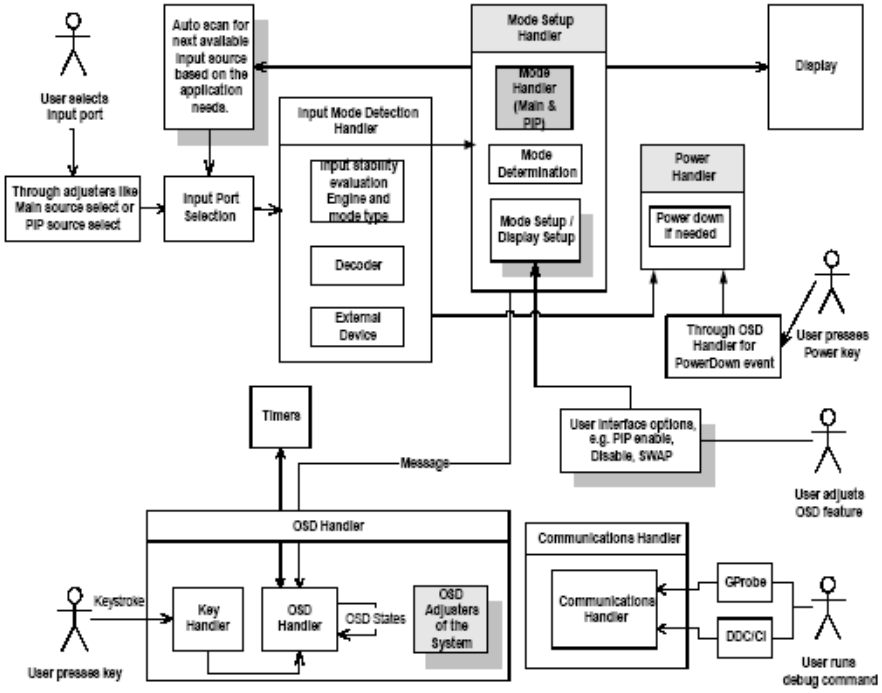


Figure 8-1 User Interface Block Diagram

The operation of keypad

There are 8 keys to control and select the function of SHD-3010 and also have two LED to indicate the status of operation. They are “Power, Source, MENU, ▼▲, + -” keys and LED.

1. The power key controls video processor FLI8532, FLI8532 will receive a low signal to turn on or off system while press the power key.
2. The other seven keys are on high state because the pull up resistor but will transit to low state dependent on which key pressed, and the state will be reader by FLI8532 through internal ADC to act corresponding function.
3. The LED is constructed with two color LED which color is Yellow and Green. The FLI8532 direct control the LED’s when FLI8532 (VPCON) is low the LED is Yellow (Close power) when FLI8532 (VPCON) is high the LED is Green (Open power).

The operation of Video Processor FLI8532

The Genesis Microchip FLI8532 includes an integrated 3-D Digital Video Decoder with Faroudja DCDi CinemaTM video format conversion, video enhancement, and noise reduction.

The auto-detection and Faroudja DCDi CinemaTM technology allow the FLI8532 to detect, process, and enhance any video or PC graphic format. The FLI8532 supports many worldwide VBI standards for applications of Teletext, Closed Captioning, V-Chip, and other VBI technologies.

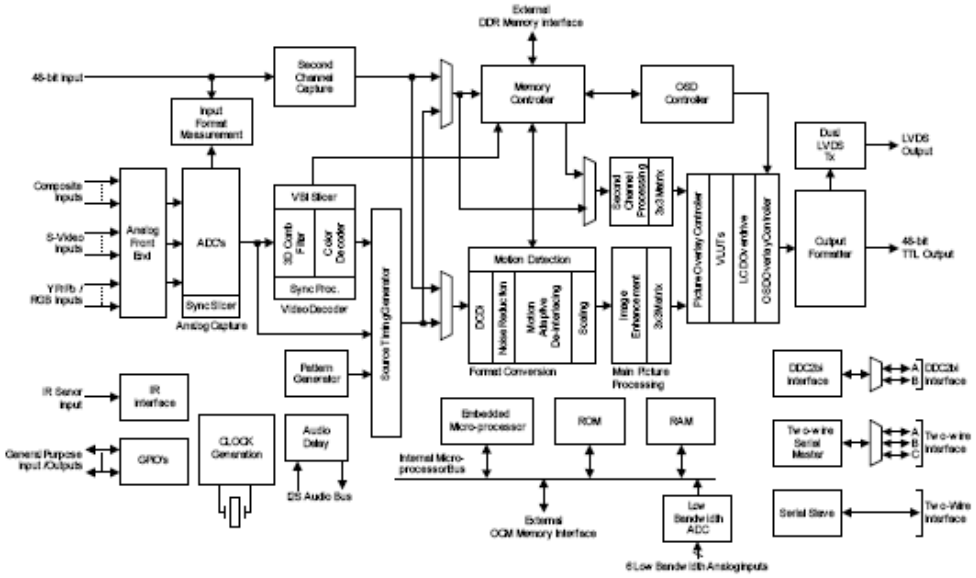


Figure 8-2 FLI8532 Block Diagram

Clock Generation:

The FLI8532 features six clock inputs. All additional clocks are internal clocks derived from one or more of these:

1. Crystal Input Clock (TCLK and XTAL). This is the input pair to an internal crystal oscillator and corresponding logic. A 19.6608 MHz TV crystal is recommended for best noise immunity with the 3D decoder. Alternatively, a single-ended TTL/CMOS clock oscillator can be driven into the TCLK pin (leave XTAL as N/C in this case). If an external crystal is being used, connect a 10K pull-up to OCMADDR_19. See Figure 9.
2. Digital Input Video/Graphics Clocks (IPCLK0, IPCLK1, IPCLK2 and IPCLK3)
3. Audio Delay Clock (AVS_CLK)

   The FLI8532 TCLK oscillator circuitry is a custom designed circuit to support the use of an external oscillator or a crystal resonator to generate a reference frequency source for the FLI8532device.

Analog Input Port (AFE):

The FLI8532 chip has a sophisticated Analog Front End with 16 reconfigurable inputs through and analog multiplexer to anti-alias filters before the Analog to Digital Converters (ADCs). These integrated features eliminate the need for any devices between the input connector and the pin of the FLI8532.

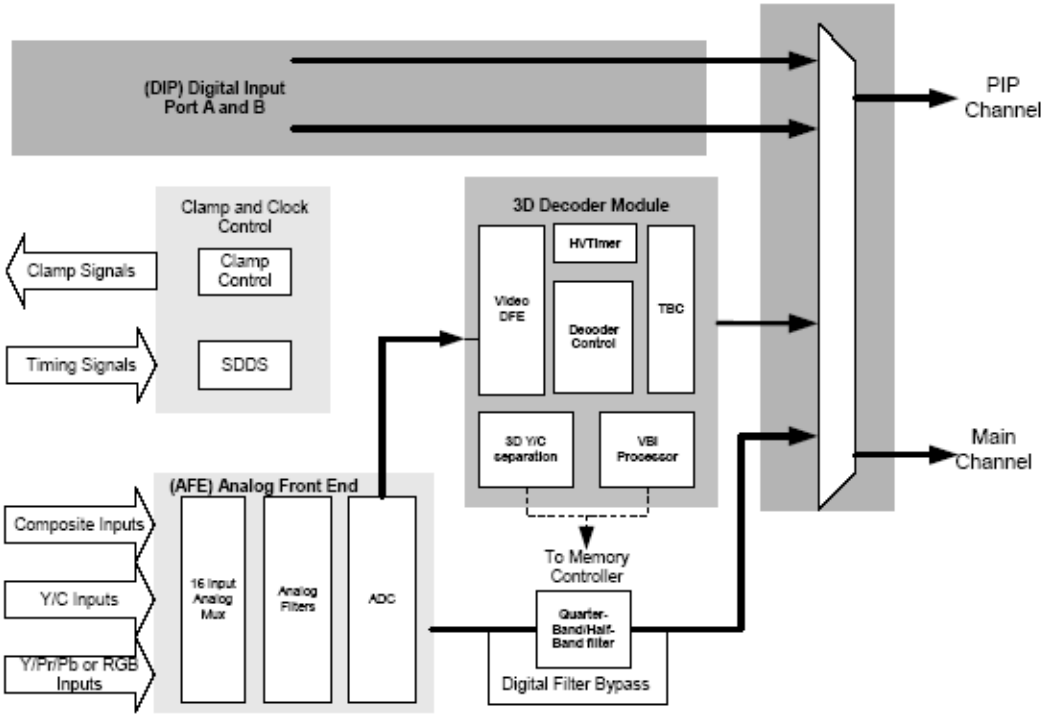


Figure 8-3 Analog Front End

The figure above depicts the data-path for the AFE and Decoder blocks with connections to the input multiplexer that selects whether the data follows the Main Video Channel or PIP video channel.

The analog front end of FLI8532 provides the capability to capture 16 analog video inputs which can be a combination of Composite (CVBS), S-Video (SY, SC), YPrPb (Y, Pr, Pb) or RGB (R,G, B).

Digital Input Port (DFE):

The Digital Input Port is a 48bit data input with flexible configuration to support a wide range of digital sources. It consists of two 24bit ports (PORTA and PORTB), two sets of control signals (VS, HS, ODD, etc.), and 4 input clocks. Up to 4 different inputs are supported as long as at least 2 of these inputs are 8bit CCIR656.

PORTA also includes optional signals (DIP_EXT_CLAMP, DIP_EXT_COAST, DIP_CLEAN_HS_OUT) for interfacing to external ADC/PLL devices. These signals are not present on PORTB. Bits 7 to 0 of PORTA can be configured as a bidirectional interface for media card applications. Inputs to the digital input port are TTL compatible with a maximum clock speed of 135MHz. Sync and clock polarity is programmable.

Due to pin sharing, PORTB is not available when using 48bit double wide TTL output to the panel.

The following digital video formats are supported by FLI8532 digital video graphic port:

- ITU-BT-656
- 8-bit 4:2:2 YCbCr or YPbPr
- 16-bit 4:2:2 YCbCr or YPbPr
- 24-bit 4:4:4 YCbCr or YPbPr
- 24-bit RGB

Digital Input Port Configuration:

The Digital Input Port offers flexible mapping of the input buses for PORTA and PORTB and allows individual Bus Flipping (MSB to LSB) for each group of 8bit inputs. The purpose of this flexible mapping is to ease the circuit board design when interfacing to other devices. This table below shows how the input DATA buses can be arbitrarily assigned through host registers.

		DIP_XX_BUS_SWAP					
Mode	**Input Bus**	"000"	"001"	"010"	"011"	"100"	"101"
24 bit RGB	DATA[7:0]	Green	Green	Blue	Blue	Red	Red
	DATA[15:8]	Blue	Red	Green	Red	Green	Blue
	DATA[23:16]	Red	Blue	Red	Green	Blue	Green
24 bit YUV	DATA[7:0]	Y	Y	U	U	V	V
	DATA[15:8]	U	V	Y	V	Y	U
	DATA[23:16]	V	U	V	Y	U	Y
16 bit YUV	DATA[7:0]	Y	Y	UV	UV		
	DATA[15:8]	UV		Y		Y	UV
	DATA[23:16]		UV		Y	UV	Y
8 bit YUV	DATA[7:0]					YUV	YUV
	DATA[15:8]		YUV		YUV		
	DATA[23:16]	YUV		YUV			

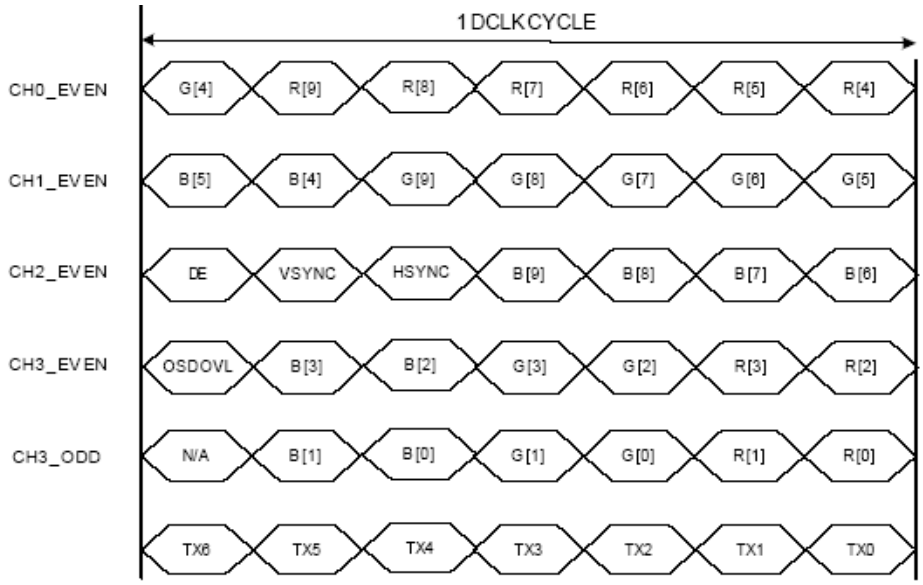
Figure 8-4 Digital Input DATA bus assignment

LVDS Transmitter:

Two LVDS channels (A and B) are available on the output of the FLI8532 to transmit data and timing information to the display device.

The following diagram shows the available LVDS mapping for 30-bit LVDS output which is applying to PDP panel spec:

30-bit LVDS Output Stream


1 DCLK CYCLE
CH0_EVEN
G[4] R[9] R[8] R[7] R[6] R[5] R[4]
CH1_EVEN
B[5] B[4] G[9] G[8] G[7] G[6] G[5]
CH2_EVEN
DE VSYNC HSYNC B[9] B[8] B[7] B[6]
CH3_EVEN
OSDOVL B[3] B[2] G[3] G[2] R[3] R[2]
CH3_ODD
N/A B[1] B[0] G[1] G[0] R[1] R[0]
TX6 TX5 TX4 TX3 TX2 TX1 TX0

To Configure for 30-bit LVDS with this data mapping:

LVDS_POWER (0x8726) = 0x3F

LVDS_DIGITAL_CTRL (0x8728) = 0bUU00UU00, where U is user options.

DISPLAY_CONTROL(0x862C)[11] = 1

For 30-bit LVDS, the following bus remappings are supported:

Swap LVDS serial stream (6:0)、(0:6) with register 0x8728[7]

Swap LVDS positive and negative differential outputs with register 0x8728[3]

Swap LVDS bus data CH0_EVEN C3_ODD and CH1_EVEN □ C3_EVEN with register 0x8728[2]

Note:

OSD OVL data bit is enabled with register 0x8500[9] with polarity controlled by 0x8500[10].

If 0x8500[9] = 0, then OSD OVL LVDS bit is clamped to 0.

On Chip Microcontroller:

The FLI8532 on-chip micro-controller (OCM) serves as the system micro-controller.

It programs the FLI8532 and manages other devices in the system such as the keypad and non-volatile RAM (NVRAM) using general-purpose input/output (GPIO) pins.

The OCM can address a 22-bit address space to utilize 4 MB external ROM

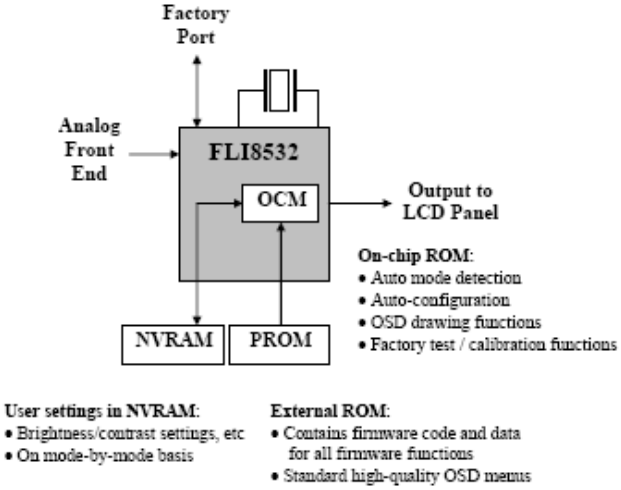


Figure 8-5 FLI8532 OCM block diagram

The OCM executes a firmware program running from external ROM, as well as driver-level (or Application Programming Interface – API) functions residing in internal ROM.

This is illustrated above. A parallel port with separate address and data busses is available for this purpose. This port connects directly to standard, commercially available ROM or programmable Flash ROM devices in either 8 or 16-bit configurations. External Flash-ROM memory requirements range from 512Kbytes to 4Mbytes depending on the application.

Both firmware and OSD content must be compiled into a HEX file and then loaded onto the external ROM. The OSD content is generated using Genesis Workbench. Genesis Workbench is a GUI based tool for defining OSD menus, navigation, and functionality.

FLI8532 I2C Master Serial Protocol :

The two-wire protocol consists of a serial clock MSTR_SCL and bi-directional serial data line MSTR_SDA. The FLI8532 acts as bus master and drives MSTR_SCL and either the master or slave can drive the MSTR_SDA line (open drain) depending on whether a read or write operation is being performed.

There are three isolated Master Serial busses, all driven by a common Master Serial Controller. These busses can be independently taken “off-line” or pulled up to different voltages without affecting the other busses.

The two-wire protocol requires each slave device to be addressable by a 7-bit identification number.

A two-wire data transfer consists of a stream of serially transmitted bytes formatted as shown in the figure below. A transfer is initiated (START) by a high-to-low transition on MSTR_SDA while MSTR_SCL is held high. A transfer is terminated by a STOP (a low-to-high transition on MSTR_SDA while MSTR_SCL is held high) or by a START (to begin another transfer).

Figure 8-6 Two-Wire Protocol Data Transfer

Each transaction on the MSTR_SDA is in integer multiples of 8 bits (i.e. bytes).

The number of bytes that can be transmitted per transfer is unrestricted. Each byte is transmitted with the most significant bit (MSB) first. After the eight data bits, the master releases the MSTR_SDA line and the receiver asserts the MSTR_SDA line low to acknowledge receipt of the data.

The master device generates the MSTR_SCL pulse during the acknowledge cycle. The addressed receiver is obliged to acknowledge each byte that has been received.

The operation of Video Processor FLI8125

FLI8125 is another video processor designed by Genesis. In this product, we use FLI8125 to process most of PIP source input and then output digital video signal to FLI8532.

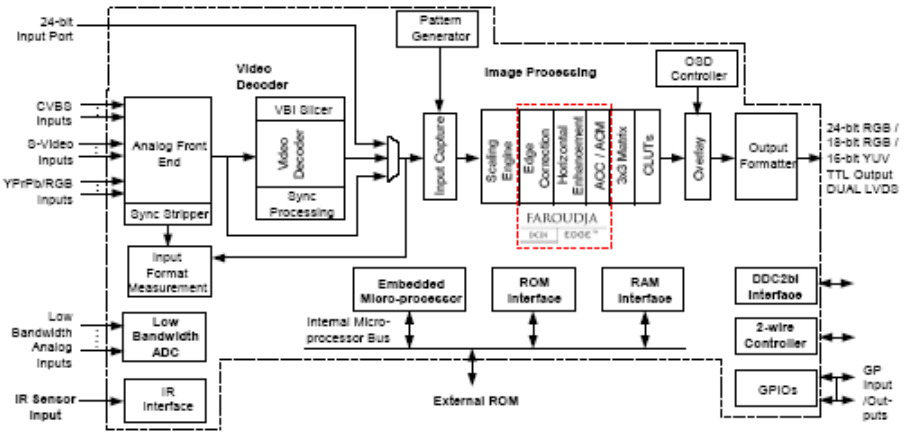


Figure 8-7 FLI8125 System Block Diagram

Clock Generation

The FLI8125 accepts the following input sources:

1. Crystal Input Clock (TCLK and XTAL). This is the input pair to an internal crystal oscillator and corresponding logic. Alternatively, a single ended TTL/CMOS clock input can be driven into the XTAL pin (leave TCLK as n/c in this case).
2. External Clocks on various GPIOs for test purposes
3. Host Interface Transfer Clock (SCL), I2C slave SCL for DDC2Bi and another SCL for Serial Inter-Processor Communication (SIPC)
4. Video Port VCLK
5. Second Video port clock. This is shared with ROM Address line 11. This is available only when parallel ROM interface is not used.

Clock Synthesis

Additional synthesized clocks using PLLs:

1. Main Timing Clock (T_CLK) is the output of the chip internal crystal oscillator. T_CLK is derived from the TCLK/XTAL pad input.
2. Reference Clock (R_CLK) synthesized by RCLK PLL using T_CLK or EXTCLK as the reference.
3. Input Source Clock (SCLK) synthesized by SDDS PLL using input HS as the reference. In case of analog composite video input this runs in open loop. The SDDS also uses the R_CLK to drive internal digital logic.
4. Display Clock (DCLK) synthesized by DDDS PLL using IP_CLK as the reference. The DDDS also uses the R_CLK to drive internal digital logic.
5. Fixed Frequency Clock (FCLK) synthesized by FDDS. Used as OCM_CLK domain driver.
6. Extended Clock (ECLK) synthesized by EDDS. Used by the decoder.
7. A fixed frequency clock created by LDDS (LCLK). Used by the expander in case of panoramic scaling.

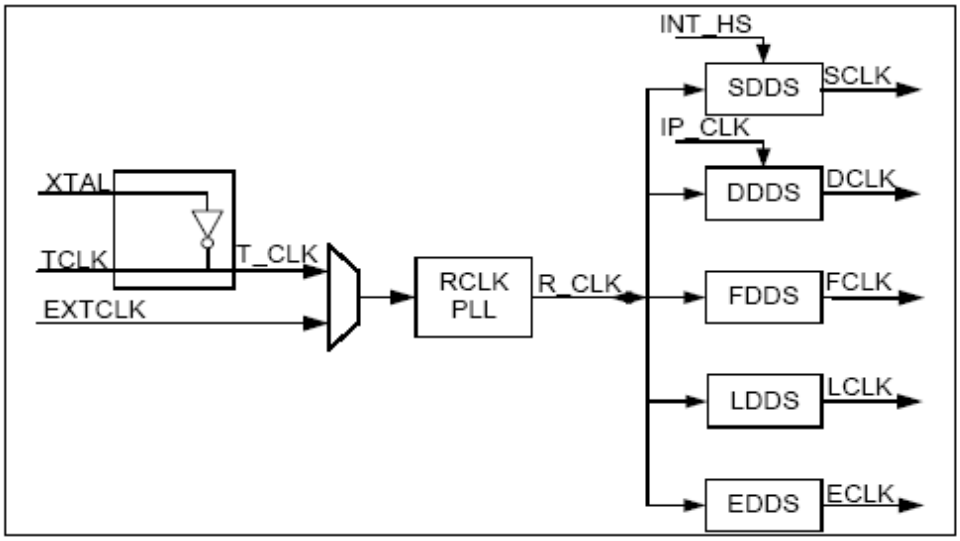


Figure 8-8 FLI8125 Internally Synthesized Clocks

Analog Front End

The Analog Front End is responsible for selecting and capturing the desired analog input video stream. Overall application cost is reduced by providing analog switching capabilities for 16 separate analog signals. These signals are re-configurable as different combinations of composite, S-Video, YPrPb and RGB video streams depending upon the end application.

The Analog Front End directs inputs through an analog multiplexer to anti-alias filters before the Analog to Digital Converters (ADCs). These integrated features eliminate the need for any devices between the input connector and the AFE pin connection.

The following figure depicts the data-path for the AFE and Decoder blocks with connections to the input multiplexer .

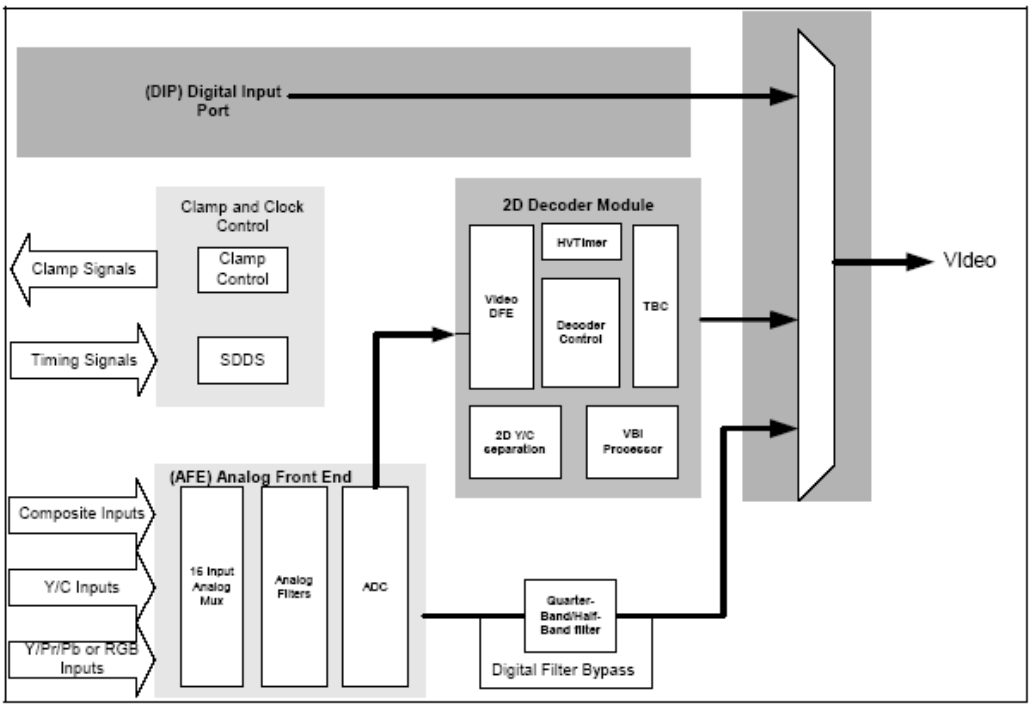


Figure 8-9 Analog Input Port

The Analog Front End provides the capability to capture 16 analog video inputs which can be a combination of Composite (CVBS), S-Video (SY, SC), YPrPb (Y, Pr, Pb) or RGB (R, G, B). The Analog Source Selectors are responsible for switching the desired analog inputs to the ADCs for digitization. There are two types of switching required: Channel Selection, Fast Blank Switching.

Digital Front End (Digital Processing after AFE)

The DFE consists of 3 channels that can support the following Fixed-position formats: Channels 1, 2 and 3 can be either R,G,B, or Y,U,V or 2 channels of Y and C or one channel of CVBS. The DFE performs Digital Clamp Loop Control for each channel, AGC Control, Color Conversion, Chroma Downscaling and 4fSC re-sampling. The Input to the DFE is 10 bit 40MHz Data. The Output is 4fsc Sampled CVBS, Y, C or YUV or just 10 bit CVBS.

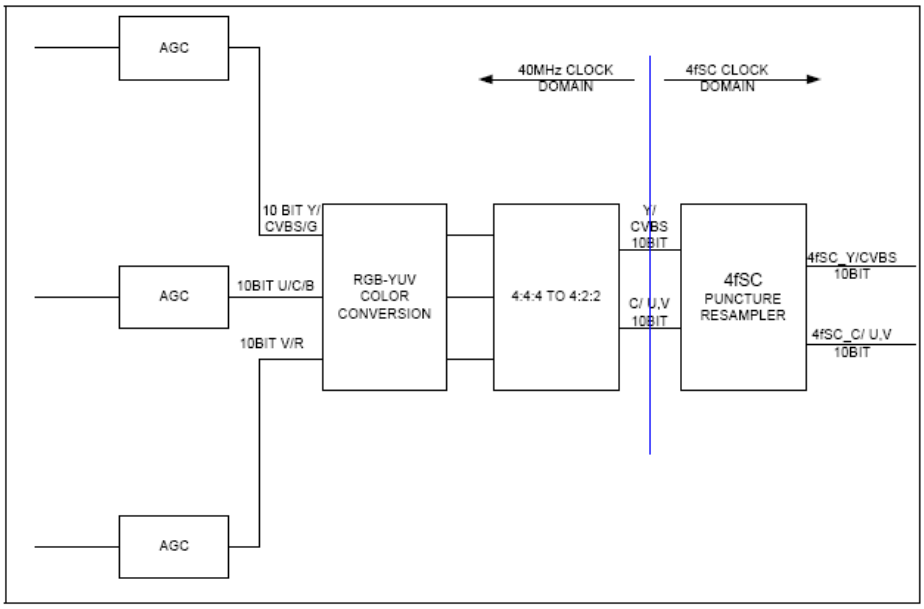


Figure 8-10 Digital Datapath

Digital Input Port

The Digital Input Port is 24-bit input bus that can be connected to external DVI receivers, video decoders, etc. and is able to accept either 8-bit CCIR656 data, 16-bit 4:2:2 YUV data or 24-bit RGB data.

For RGB input data, a selectable color space converter is used to transform RGB video input data from a DVI Rx to internal 16-bit 4:2:2 YUV. This allows the input data to be processed by the Horizontal Enhancment Module (HEM), ACC, and ACM in the image processing block. Other RGB input data streams, such as computer inputs, remain in the RGB space and are processed as such.

The 24-bit Digital Input Port provides control signals to simplify signal detection. CCIR656 data streams embedd all timing markers, for the 24-bit and 16-bit inputs the following signals are provided:

- CLK1 – Input pixel clock for 24-bit, 16-bit or CCIR656 inputs
- HS/CSYNC – Horizontal sync or composite sync signal
- VS/SOG – Vertical sync input or SOG input
- DV/CLAMP – Data valid input indicator

NOTE: Unused pins of the Digital Input Port can be reprogrammed as GPIOs to increase the total number of GPIOs available.

Inputs to the digital input port are TTL compatible with a maximum clock speed of 135MHz. Sync and clock polarity is programmable.

Input Capture

The Input Capture block is responsible for extracting valid data from the input data stream and creating the required synchronization signals required by the data pipeline. This block also provides stable timing when no stable input timing exists.

The selected input data stream is cropped using a programmable input capture window. Only data within the programmable window is allowed through the data pipeline for subsequent processing. Data that lies outside of the window is ignored.

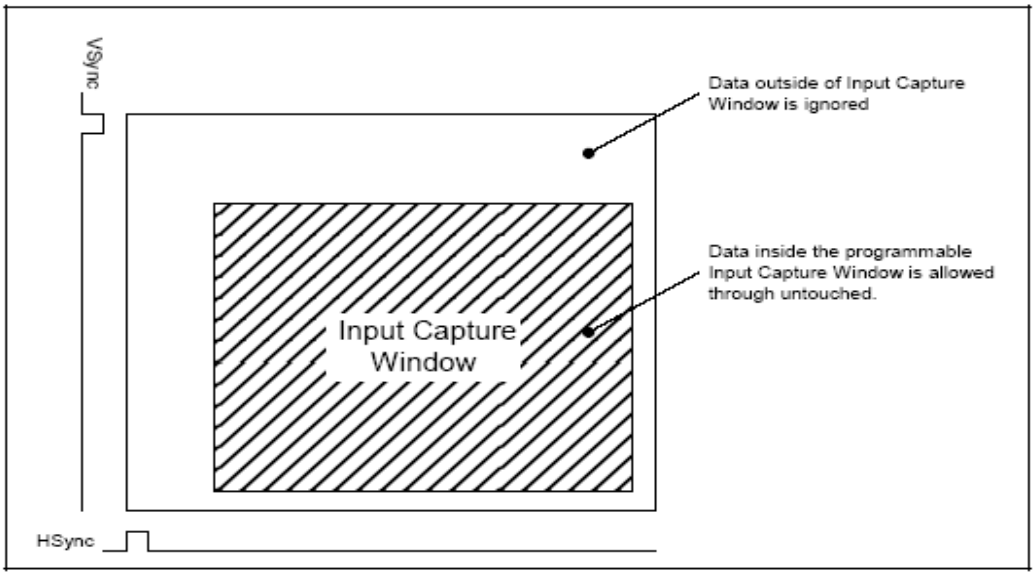

VSync
Data outside of Input Capture Window is ignored
Data inside the programmable Input Capture Window is allowed through untouched.
Input Capture Window
HSync

Figure 8-11 Input Capture Window

Input cropping is required in a video system since video signals are normally over scanned. For a flat panel TV, in order to over scan the image, a smaller portion of the input image needs to be selected and then expanded to fill the entire screen.

Input data streams originating from CCIR656 sources are cropped with reference to the start and end of active video flags encoded into the data stream. For all other inputs, the Input Capture Window is referenced with respect to Horizontal and Vertical Sync.

Image Processing

The following figure shows the various image processing blocks that operate on the captured video data stream. Each block is individually selectable and can be removed from the processing chain via a selectable bypass path. When a processing block is bypassed, it automatically enters a low power mode to help reduce overall power consumption.

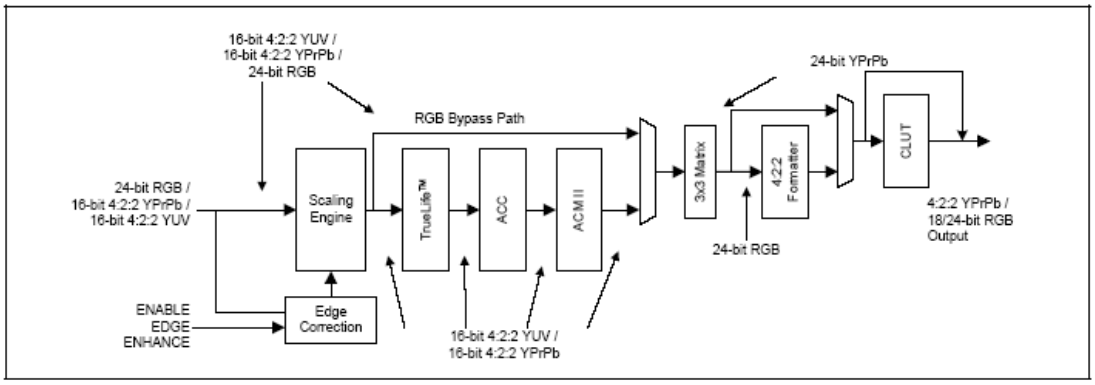


Figure 8-12 Imange Processing Block Diagram

Faroudja DCDi Edge Processing

Faroudja DCDi Edge processing is used to reduced/eliminate objectionable stair stepping that occurs on interlaced diagonal lines. DCDi Edge processing is optimized for a memory architecture that is unified with the memory used for scaling. This block can process 24-bit RGB, 16-bit 4:2:2 YUV or 16-bit 4:2:2 YPrPb data streams.

Scaling Engine

The Scaling Engine accepts both 16-bit 4:2:2 YUV and 24-bit RGB inputs. It is capable of scaling the input by a factor of 0.05 to 5.0. A flexible tap structure is used so that the number of taps can be increased based on the number of pixels per line and whether the input is 4:2:2 YUV or 4:4:4 RGB. To reduce the amount of memory required for the vertical scaling process, horizontal shrink is performed prior to vertical scaling and horizontal expansion happens after vertical scaling. The maximum number of pixels per line supported by the vertical scalar is 1366.

Display Output Interface

The Display Output Port provides data and control signals that permit the connection to a variety of flat panel devices using a 24-bit TTL or LVDS interface. The output interface is configurable for single or dual wide LVDS in 18 or 24-bit RGB pixels format. All display data and timing signals are synchronous with the DCLK display clock. The integrated LVDS transmitter is programmable to allow the data and control signals to be mapped into any sequence depending on the specified receiver format. DC balanced operation is supported as described in the Open LDI standard. Output timing is fully programmable via the host interface register set enabling this device to be used as a display controller of a PIP processor for other Genesis Microchip devices.

The following display synchronization modes are supported: Frame Sync Mode: The display frame rate is synchronized to the input frame or field rate. This mode is used for standard operation. Free Run Mode: No synchronization. This mode is used when there is no valid input timing (i.e. to display OSD messages or a splash screen) or for testing purposes. In free-run mode, the display timing is determined only by the values programmed into the display window and timing registers.

Display Timing Programming

Horizontal values are programmed in single-pixel increments relative to the leading edge of the horizontal sync signal. Vertical values are programmed in line increments relative to the leading edge of the vertical sync signal.

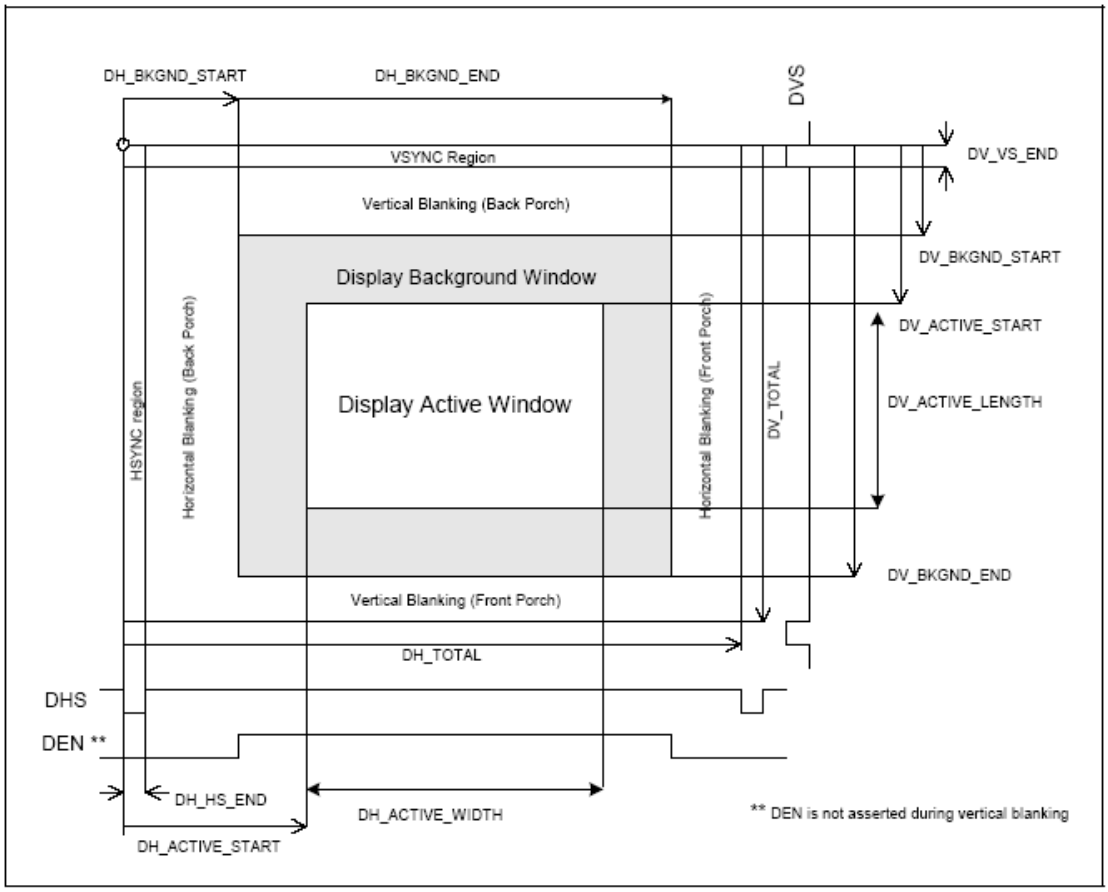


Figure 8-13 Display Windows and Timing

Data captured by the Input Capture Window and processed by the various image manipulation blocks is output in the Display Active Window. This window is always in the foreground and lies on top of all other output windows, except OSD overlay windows.

Typically the Display Active Window is set to the same size as the output of the Scaling Engine. If the Display Active Window is set too small, then the bottom and right hand edges of the image data are cropped. If the Display Active Window is set too large, then the extra space to the left and bottom of the Display Active Window is forced to the Background Window color.

Output Dithering The CLUT outputs a 10-bit value for each color channel. This value is dithered down to either 8-bits for 24-bit per pixel panels, or 6-bits for 18-bit per pixel panels. In this way it is possible to display 16.7 million colors on a LCD panel with 6-bit column drivers.

The benefit of dithering is that the eye tends to average neighboring pixels and a smooth image free of contours is perceived. Dithering works by spreading the quantization error over neighboring pixels both spatially and temporally. Two dithering algorithms are available: random or ordered dithering. Ordered dithering is recommended when driving a 6-bit panel. All gray scales are available on the panel output whether using 8-bit panel (dithering from 10 to 8 bits per pixel) or using 6-bit panel (dithering from 10 down to 6 bits per pixel).

Dual Channel LVDS Transmitter

An integrated LVDS transmitter with programmable input to output configuration is provided to enable drive of all known panels. The LVDS transmitter can support the following:

- Single pixel mode 24-bit panel mapping to the LVDS channels
- 18-bit panel mapping to the LVDS channels
- Programmable channel swapping (the clocks are fixed)
- Programmable channel polarity swapping
- Supports up to SXGA 75Hz output

On-Chip Microcontroller (OCM)

The on-chip microcontroller (OCM) is a 16-bit x86 100MHz processor capable of acting as either the overall system controller or a slave controller, receiving commands from an external controller.

The OCM executes firmware running from external ROM, as well as driver-level (or Application Programming Interface – API) functions residing in internal ROM. A parallel port with separate address and data busses is available for this purpose.

This port connects directly to standard, commercially available ROM or programmable FLASH ROM devices. A serial FLASH ROM may be used with the serial peripheral interface (SPI) and cache controller inside the Genesis device. Both firmware and OSD content must be compiled into a HEX file and then loaded onto the external ROM.

The OSD content is generated using Genesis Workbench. Genesis Workbench is a GUI based tool for defining OSD menus, navigation, and functionality.

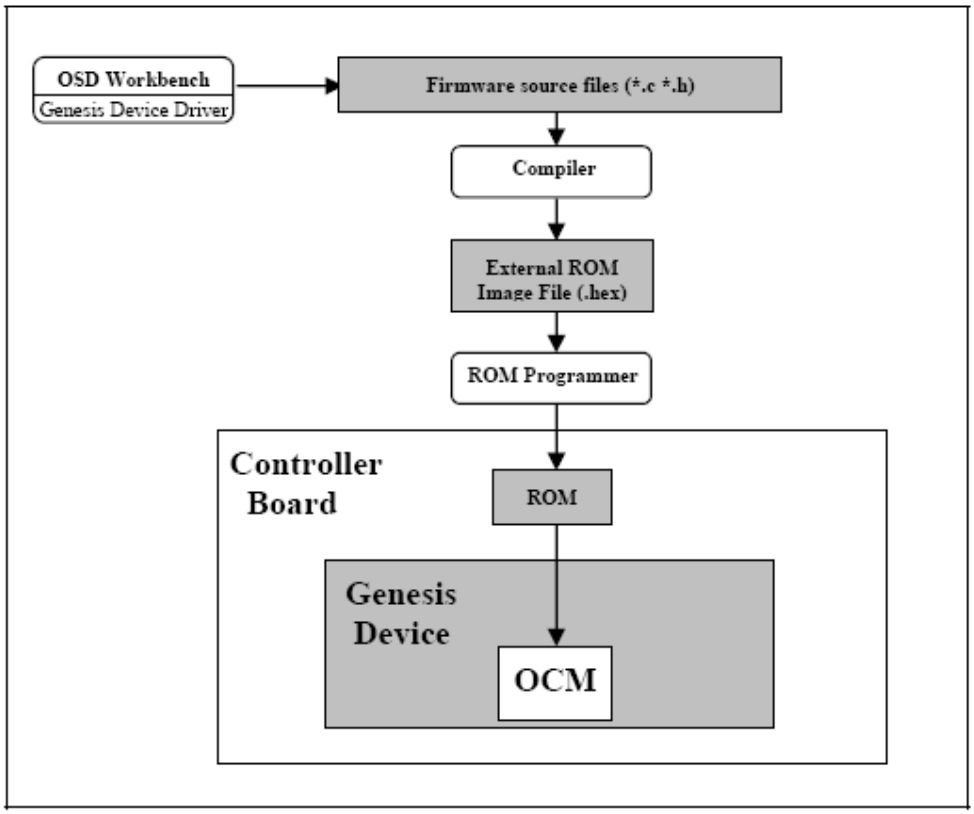
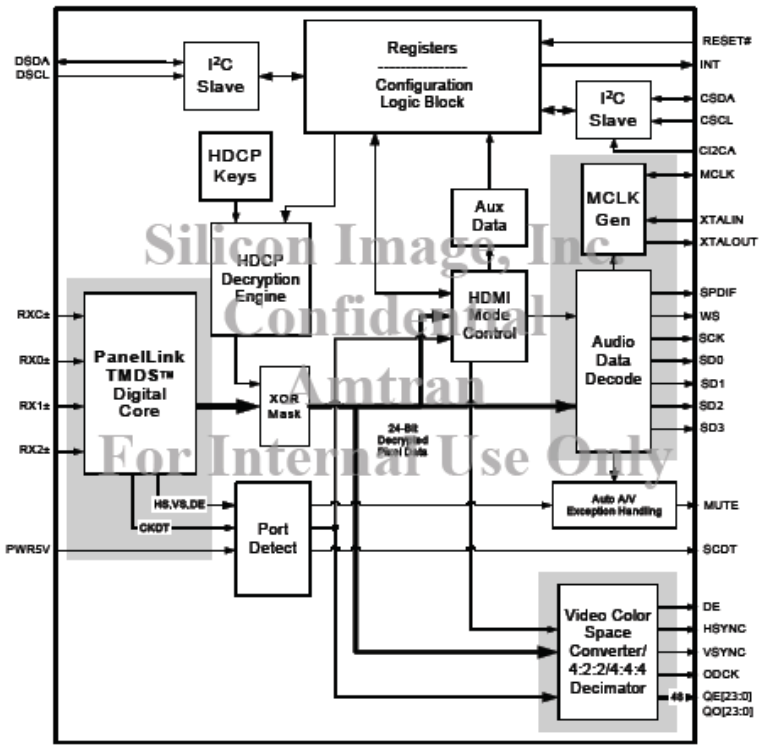


Figure 8-14 FLI8125 OCM Programming

The operation of HDMI Sil9011

The Sil 9011 provides one HDMI input port. The Sil 9011 video output goes to a video processor while the audio output goes to an audio DAC.



Silicon Image, Inc.
Confidential
Amtran
For Internal Use Only

Figure 8-15 HDMI 9011 Block Diagram

TMDS Digital Core

The core performs 10-to-8-bit TMDS decoding on the audio and video data received from the three TMDS differential data lines along with a TMDS differential clock. The TMDS core supports link clock rates to 165MHz, including CE modes to 720p/1080i/1080p and PC modes to XGA, SXGA and UXGA.

Active Port Detection

The PanelLink core detects an active TMDS clock and detects an actively toggling DE signal. These states are accessible in register bits, useful for monitoring the status of the HDMI input or for automatically powering down the receiver.

The +5V supply from the HDMI connector is used as a cable detect indicator. The SiI 9011 can monitor the presence of this +5V supply and, if and when necessary, provide a fast audio mute without pops when it senses the HDMI cable pulled. The microcontroller can also poll registers in the SiI9011 to check whether an HDMI cable is connected.

Data Input and Conversion

Mode Control Logic

The mode control logic determines if the decrypted data is video, audio or auxiliary information, and directs it to the appropriate logic block.

Video Data Conversion and Video Output

The SiI 9011 can output video in many different formats (see examples in Table 2). The receiver can also process the video data before it is output, as shown in Figure 5. Each of the processing blocks may be bypassed by setting the appropriate register bits. (See page 38 for a more detailed path diagram.)

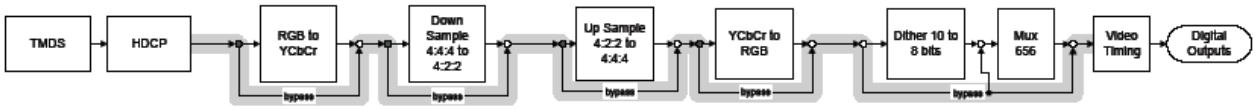


Figure 8-16 HDMI Video Processing Path

Color Range Scaling

The color range depends on the video format, according to the CEA-861B specification. In some applications the 8-bit input range uses the entire span of 0x00 (0) to 0xFF (255) values. In other applications the range is scaled narrower. The receiver cannot detect the incoming video data range, and there is no required range specification in the HDMI AVI packet.

Therefore the receiver's firmware will have to program the scaling depending on the detected video format. Refer to the SiI 9011 Programmer's Reference (SiI-PR-0006) for more details. When the receiver outputs embedded syncs (SAV/EAV codes), it also limits the YCbCr output values to 1 to 254.

For Internal Use Only

Digital Video Output Formats

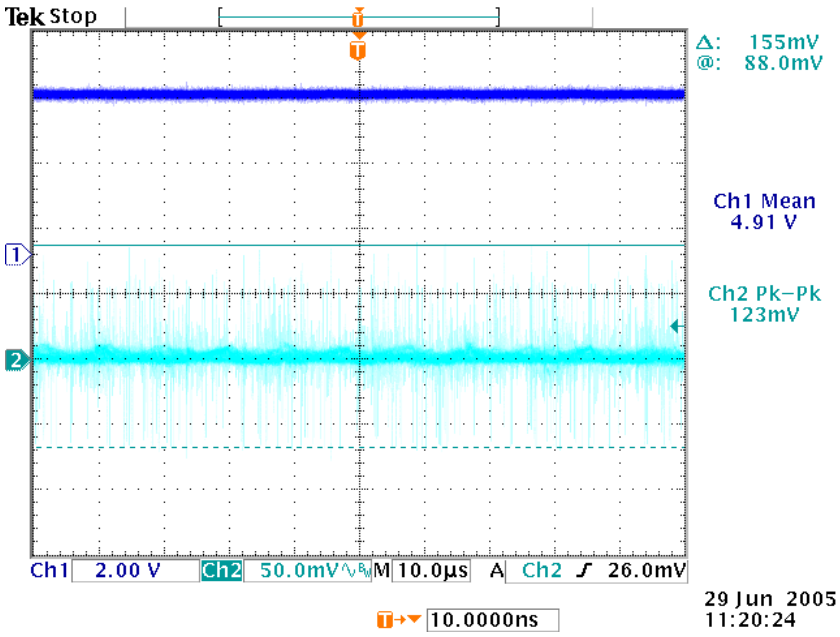
Color Space	Video Format	Bus Width	HSYNC / VSYNC	Output Clock (MHz)[3]							Notes
				480i	480p	XGA	720p	1080i	1080p	UXGA	
RGB	4:4:4	24	Separate	13.25 / 27	27	65	74.25	74.25	148.5	162	
YCbCr	4:4:4	24	Separate	13.25 / 27	27	65	74.25	74.25	148.5	162	
YCbCr	4:2:2	16/20/24	Sep, Emb.	13.25 / 27	27	—	74.25	74.25	148.5	162	1,2
YCbCr	4:2:2	8/10/12	Sep, Emb.	27	54	135	148.5	148.5	—	—	1,4
RGB	4:4:4	48	Separate	6.73/13.5	13.5	32.25	37.13	37.13	74.25	81	5
YCbCr	4:4:4	48	Separate	6.73/13.5	13.5	32.25	37.13	37.13	74.25	81	5
RGB	4:4:4	12	Separate	13.25 / 27	27	65	74.25	74.25	—	—	6
YCbCr	4:4:4	12	Separate	13.25 / 27	27	65	74.25	74.25	—	—	6
YCbCr	4:2:2	8/10/12	Sep, Emb.	13.25/27	27	65	74.25	74.25	—	81	1,4

Figure 8-17 Digital Video Output Formats

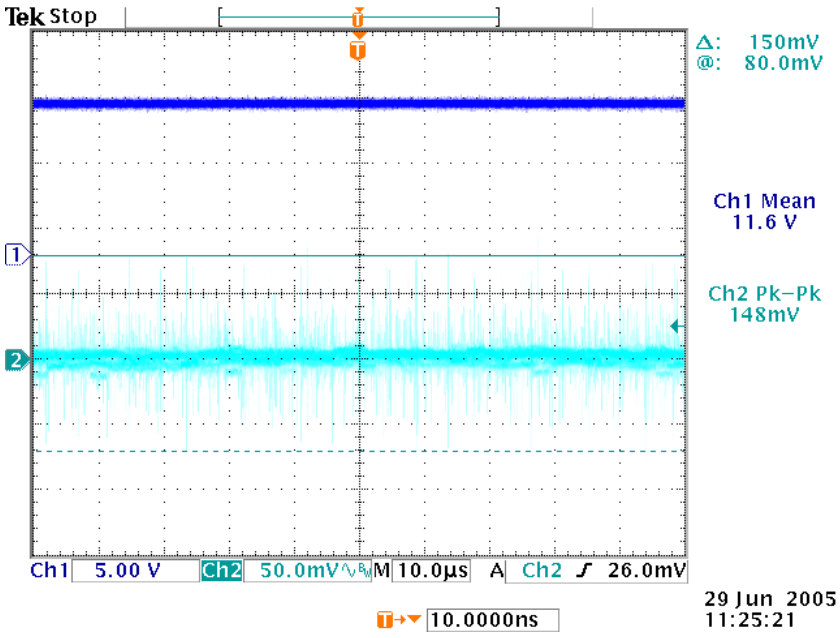
Chapter 9 Waveforms

1. Ripple Voltage

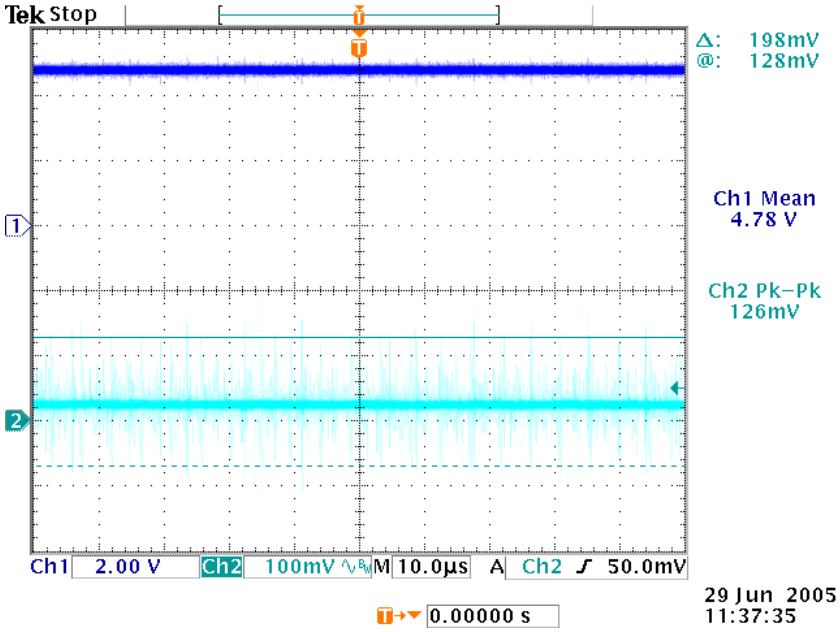
(1) PDP_+5Vsc (CN1.1)



(2) PDP_+12V (CN1.7)

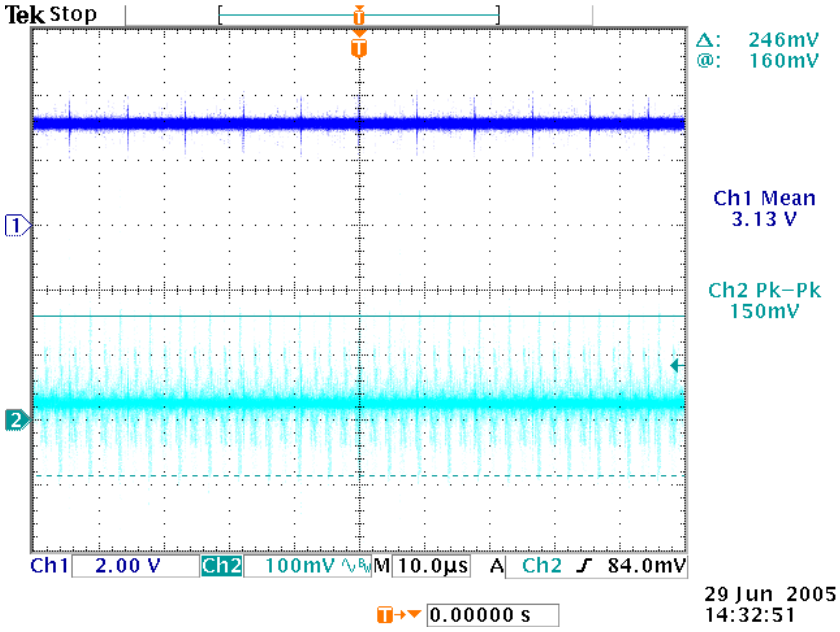


(3) PDP_+5Vsb (CN3.4)

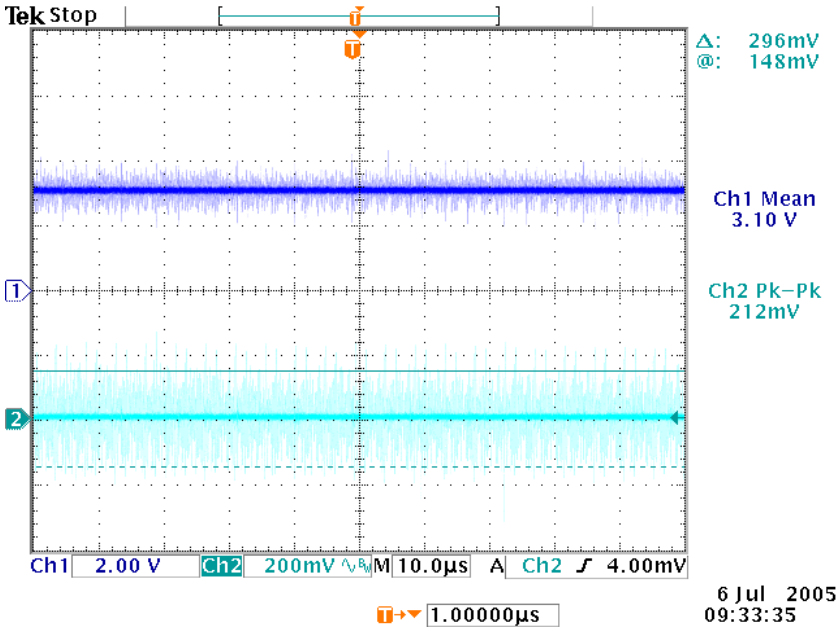


(4) FLI8125 (U10)

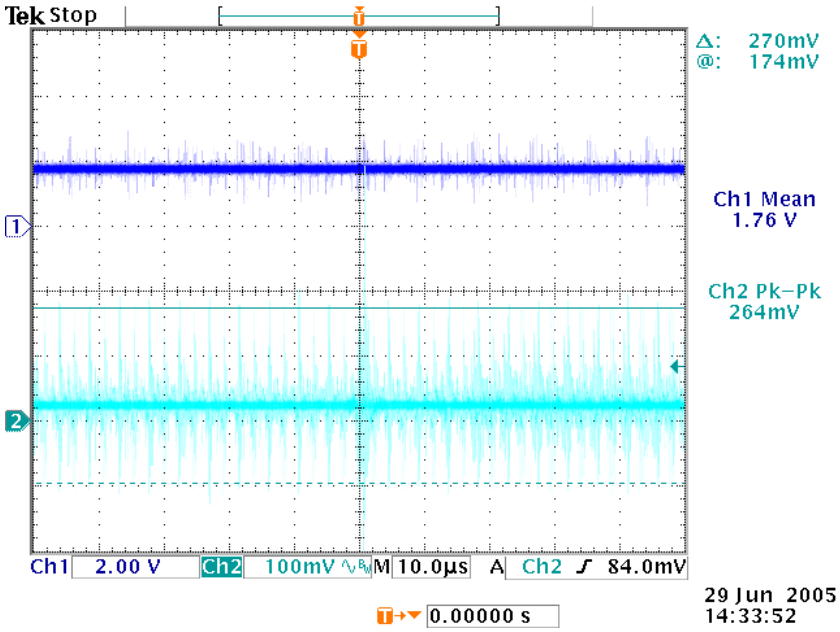
+3.3V_I/O_HUD



+3.3V_ADC_HUD

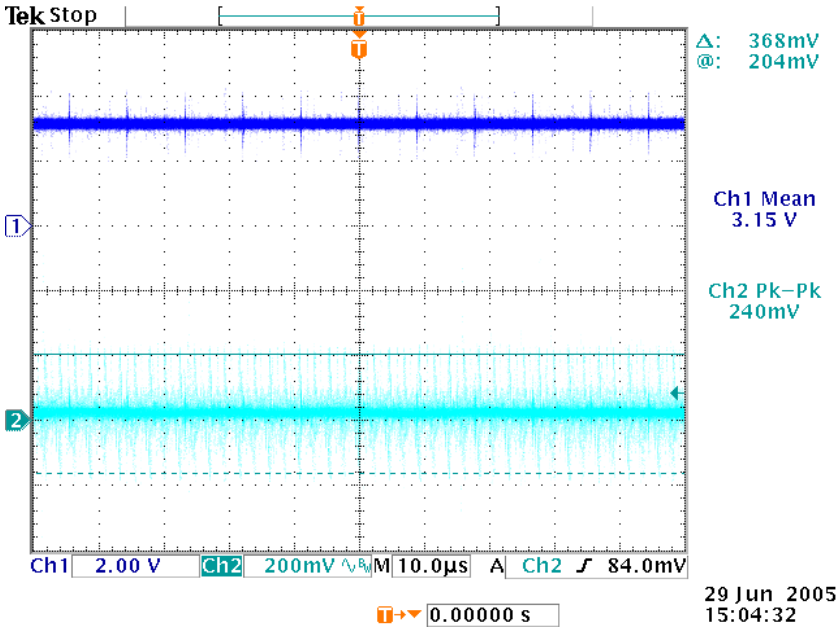


+1.8V_ADC_HUD

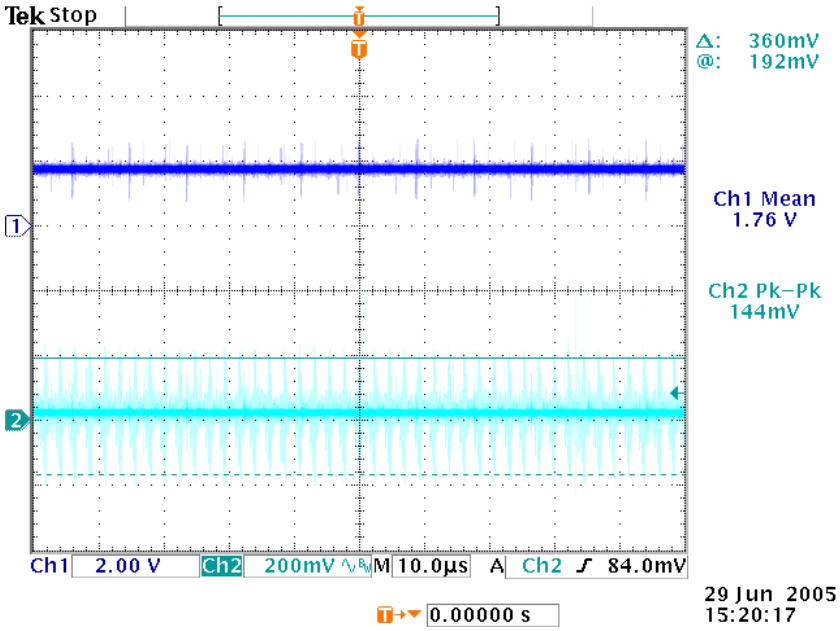


(5) FLI8532 (U13)

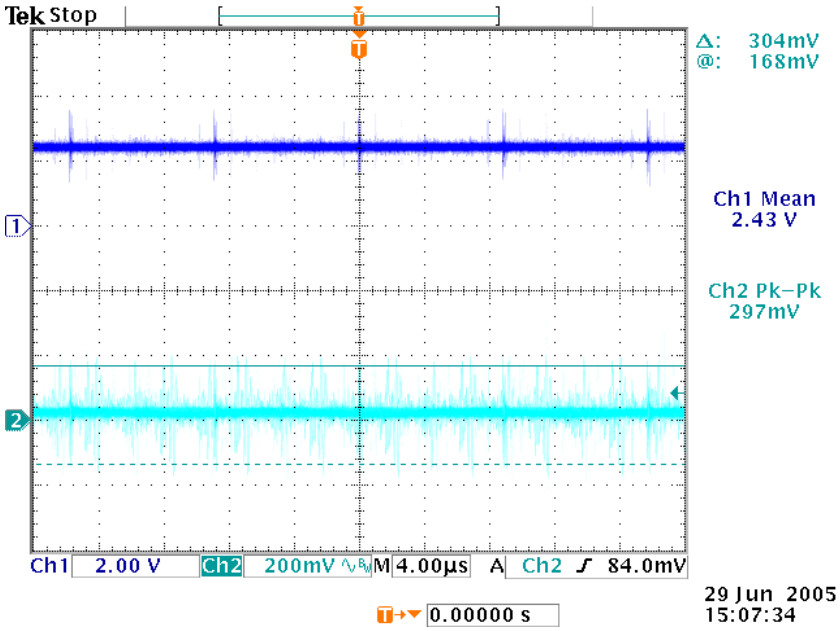
+3.3V_I/O



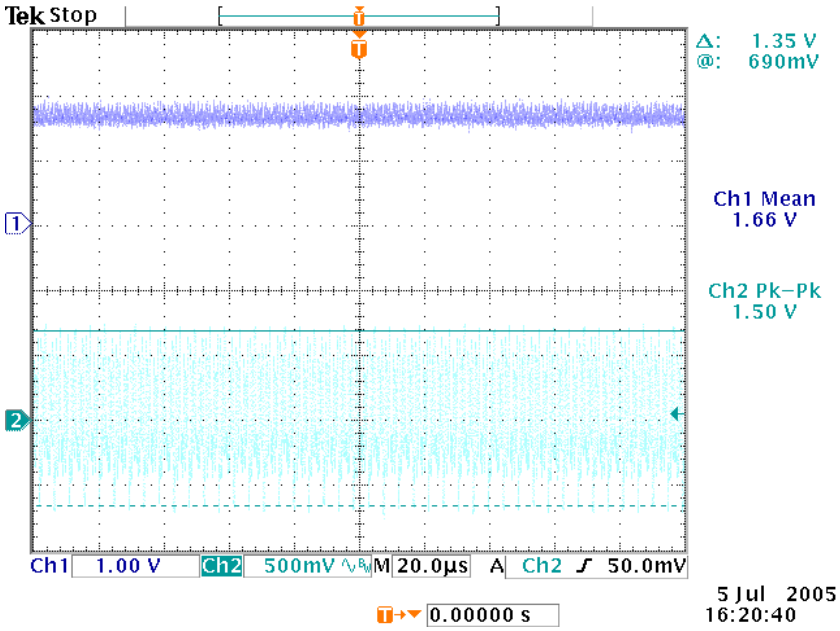
+1.8V_ADC



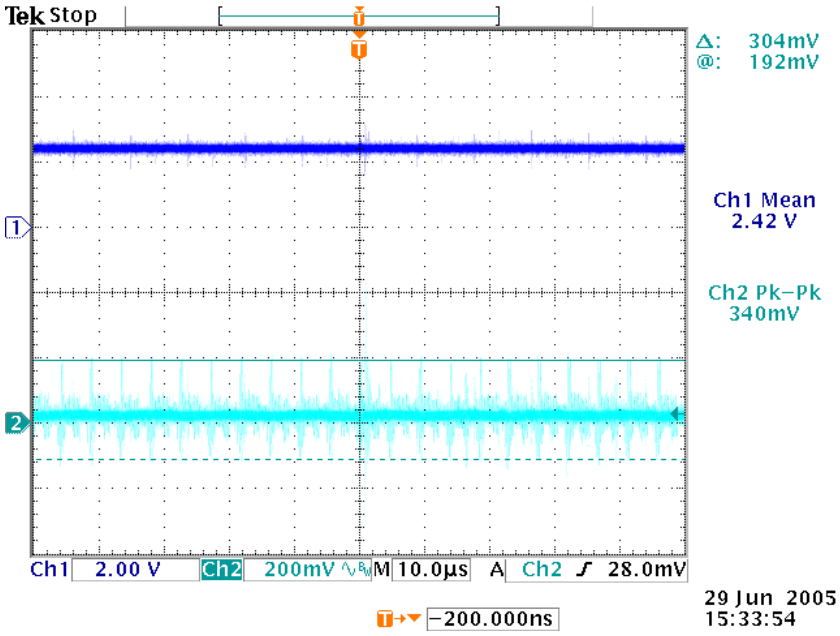
+2.5V_DDR



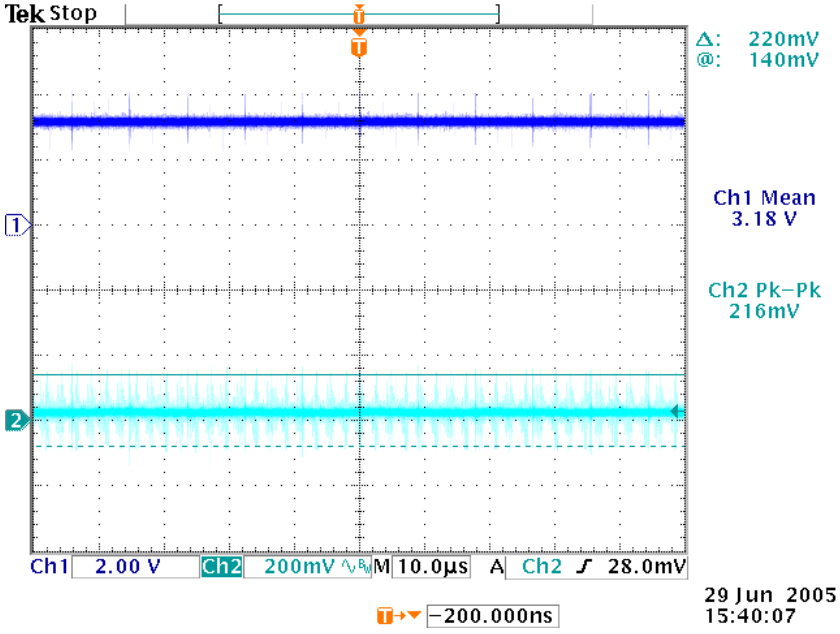
+1.8V_CORE



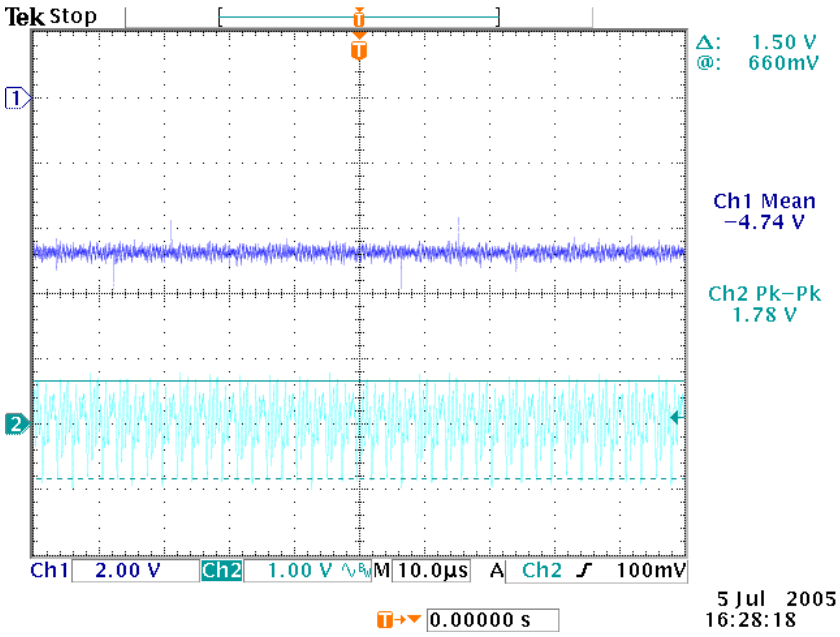
(6) NT5DS16M16CS-5T (U16, U17)



(7) Am29LV320DT90-ED (XU1)

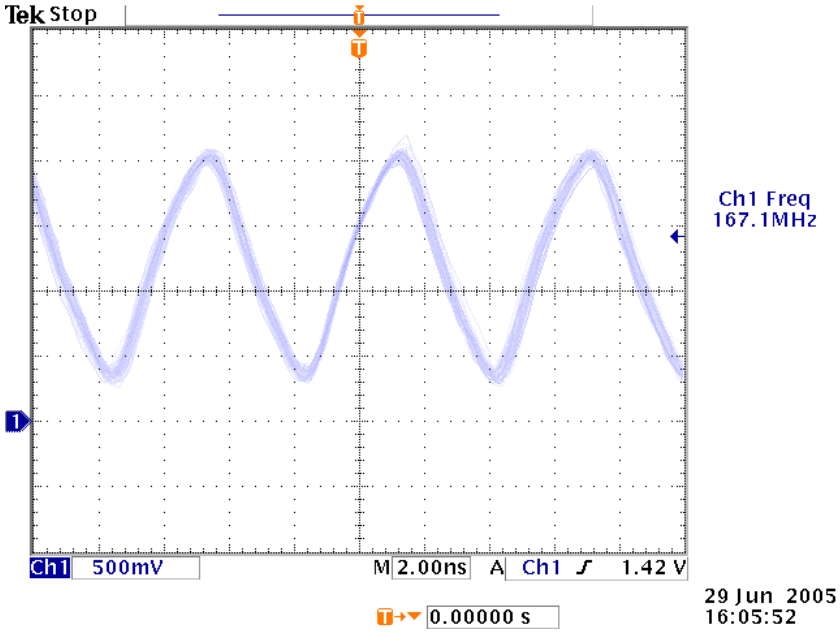


(8) LM2660 (-5V_N of the U29)



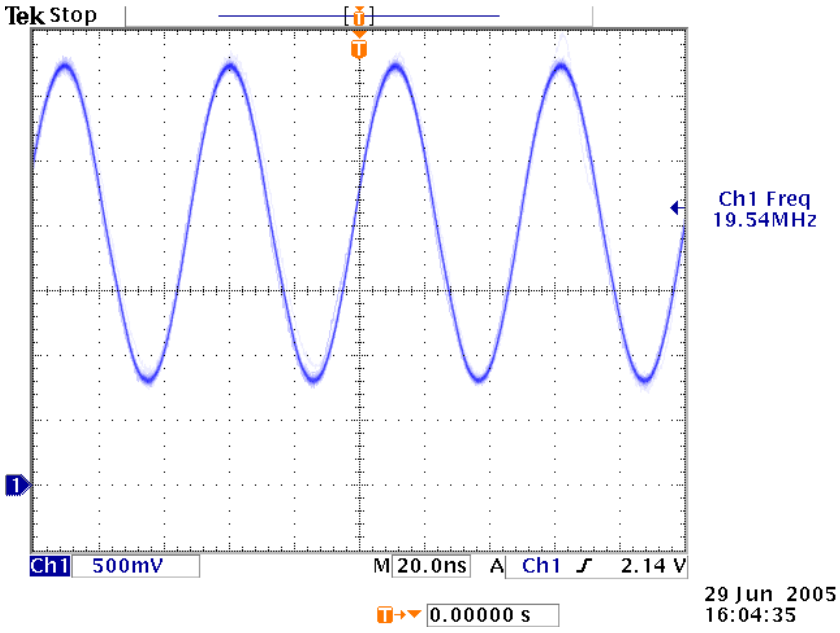
2. Clock Timing

(1) NT5DS16M16CS-5T DDR clock (pin 45 of the U16 or U17)

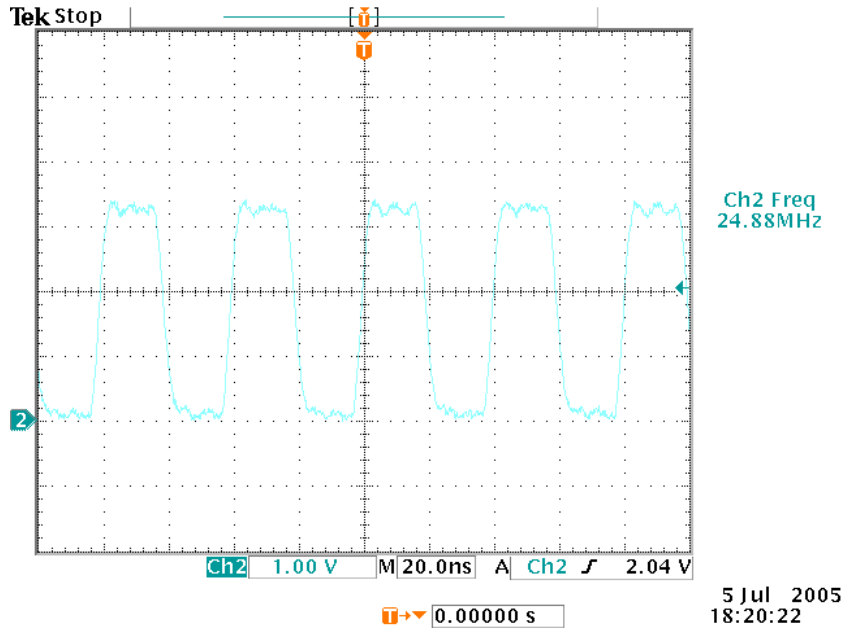


(2) FLI8125

Crystal clock (pin 15 of the U10)

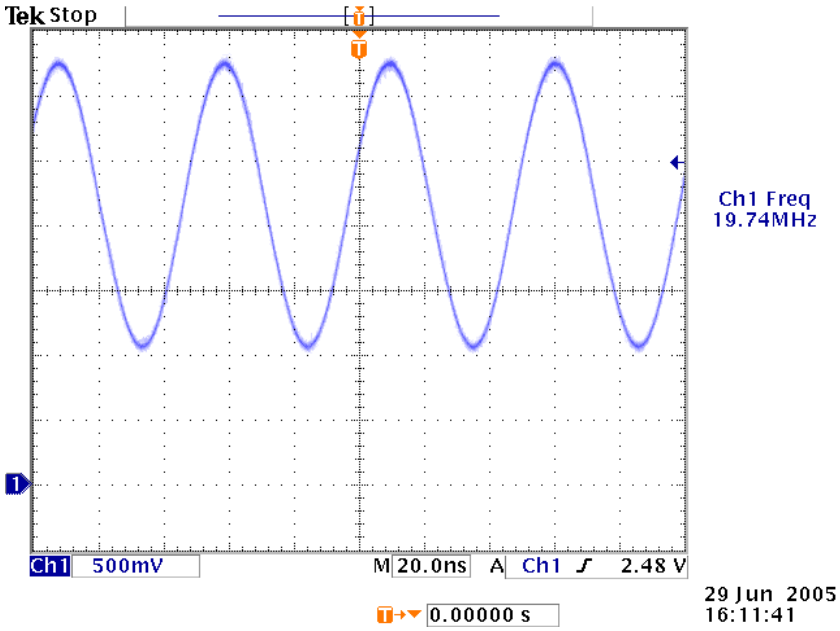


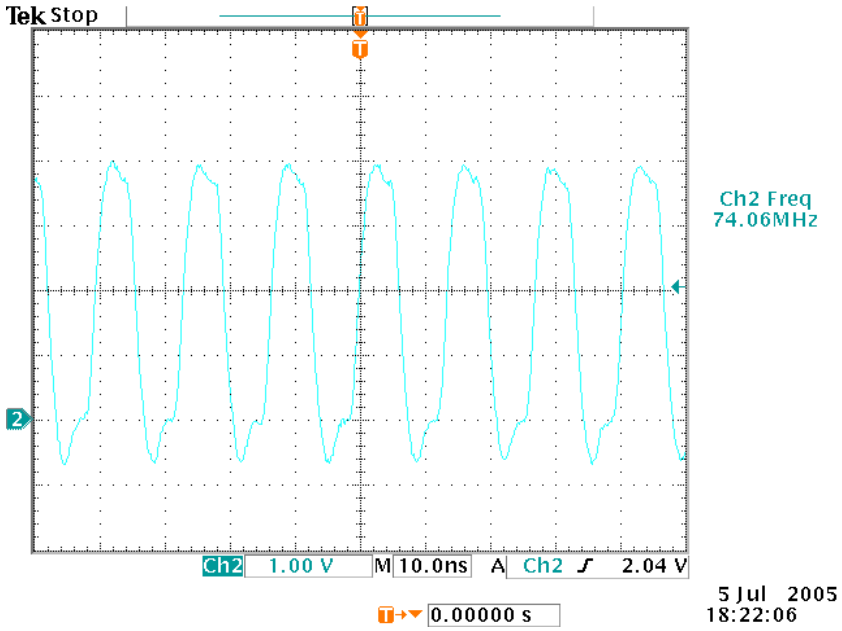
Hudson output clock



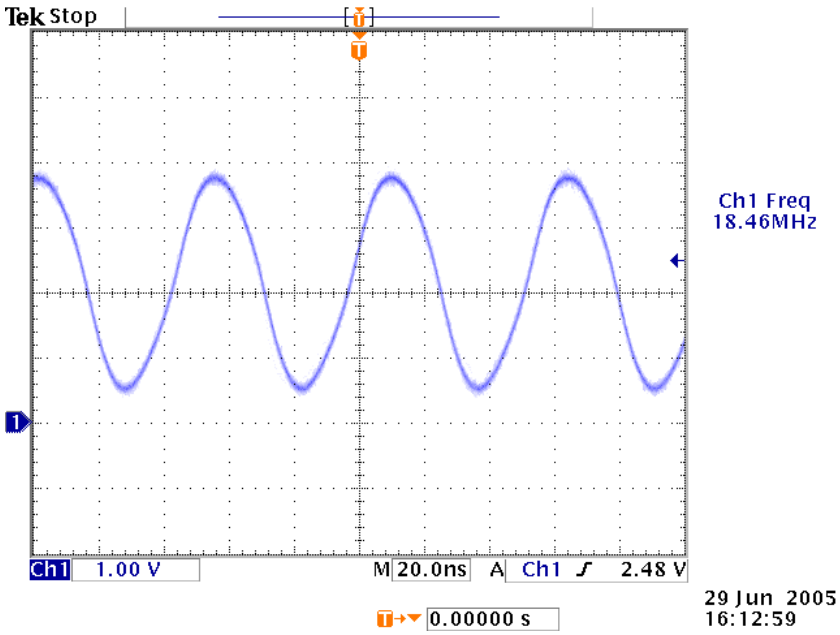
(3) FLI8532

Crystal clock (pin B26 of the U13 or pin 1 of the C155) Cortze output clock

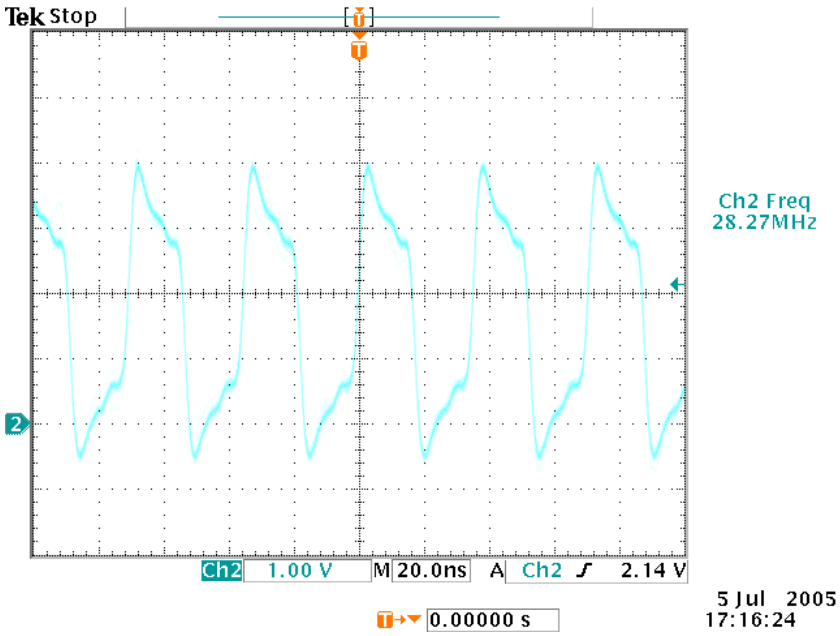




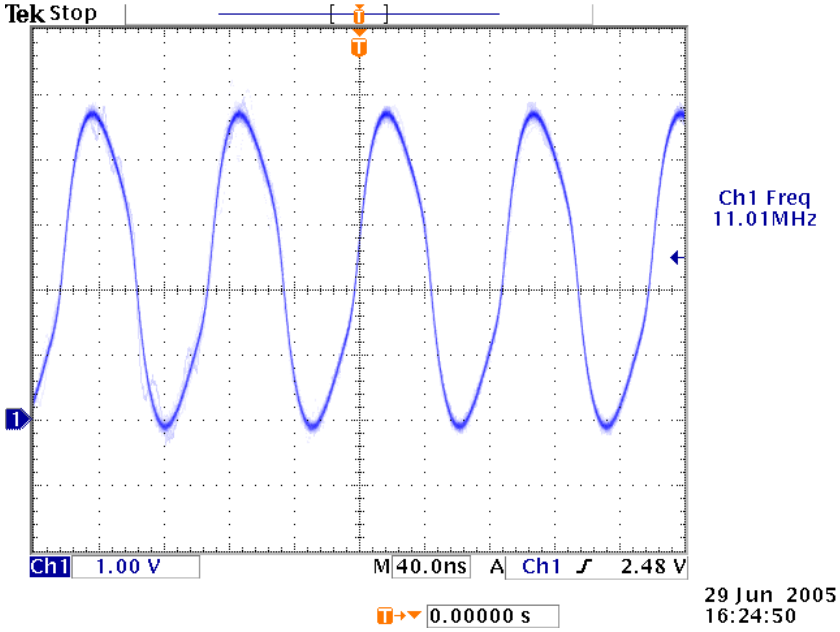
(4) MSP4450G crystal clock (pin 55 of the U32)



(5) Sil9011CLU crystal clock (pin 84 of the U35 and U42)



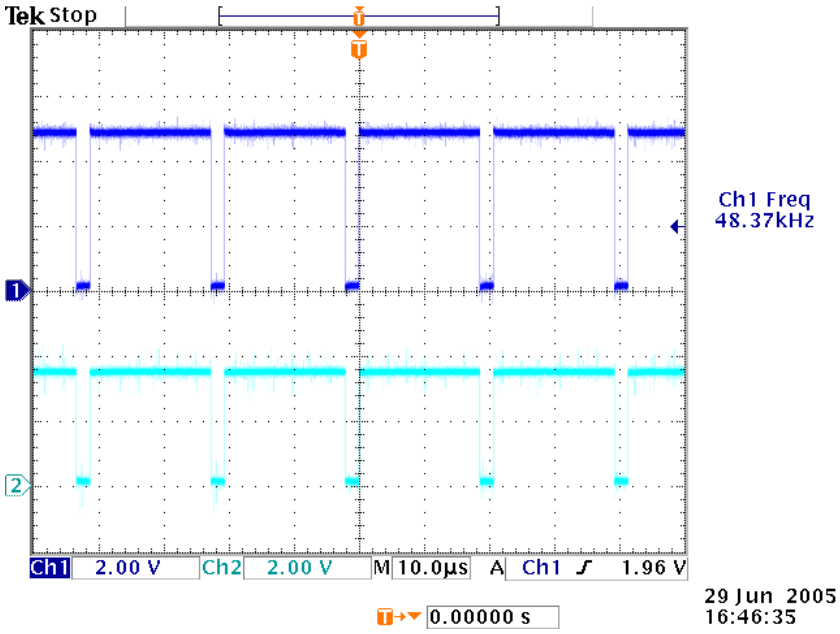
(6) IC SM5964C40J crystal clock (pin 20 of the U38)

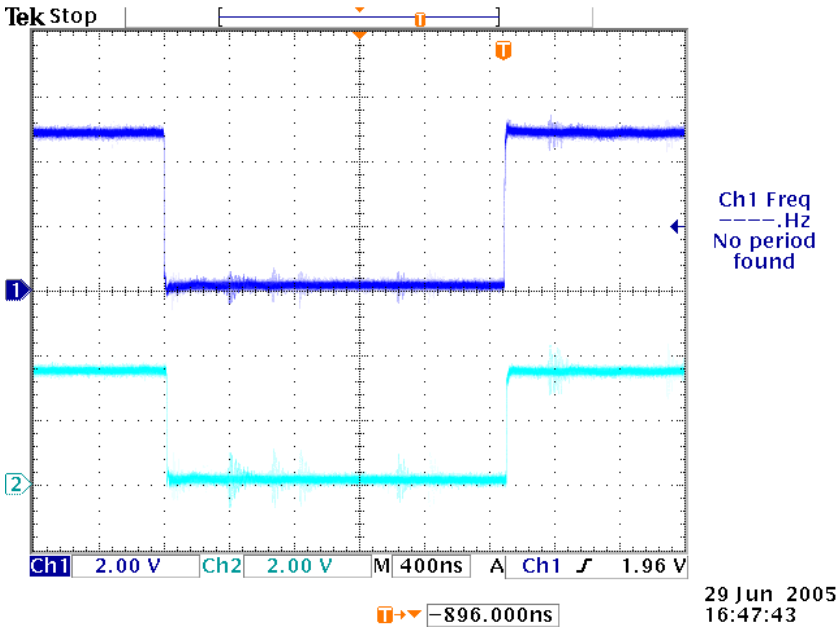


3. Horizontal and Vertical sync. Timing

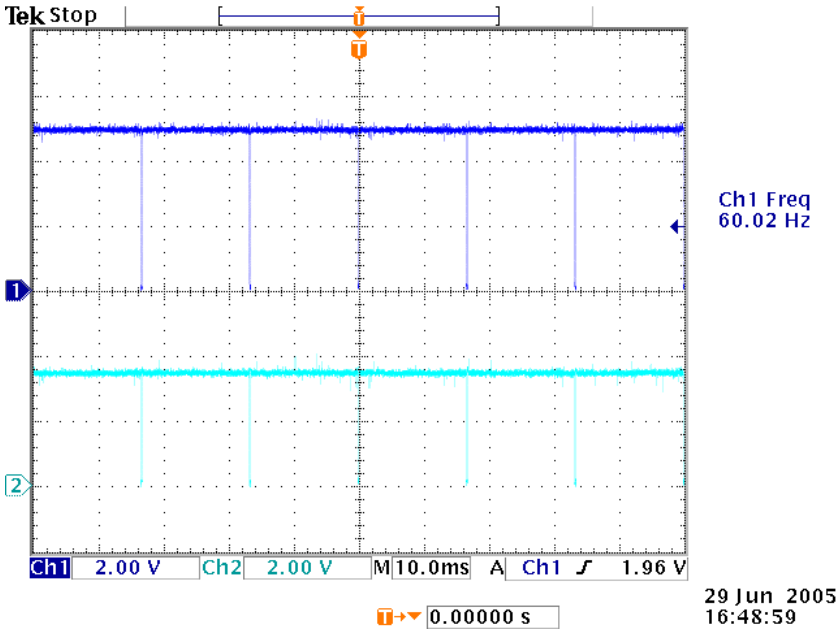
(1) VGA input (1024x768x60Hz)

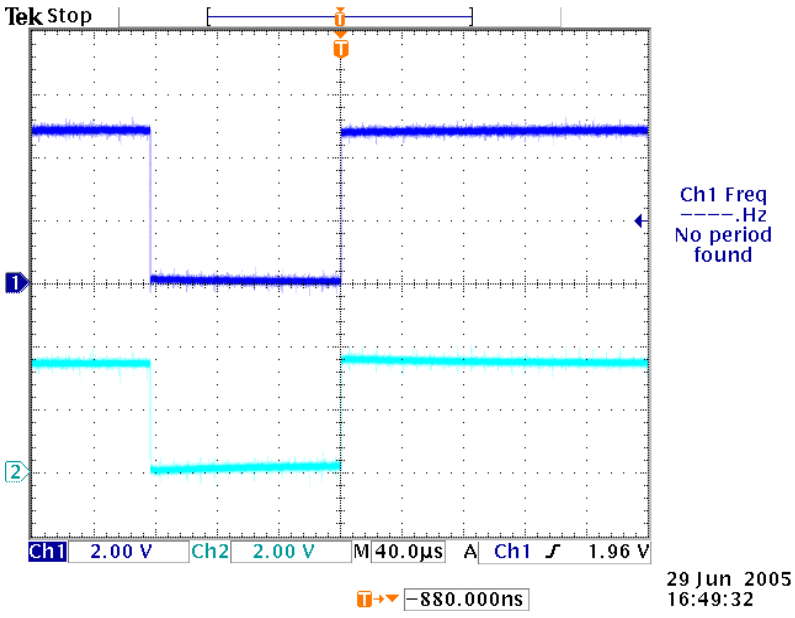
H-sync





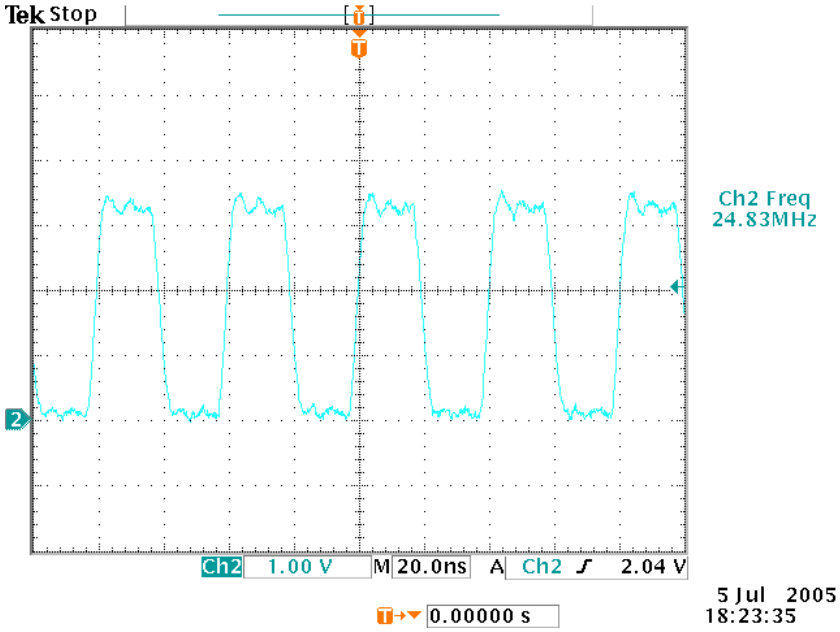
V-sync


Tek Stop
Ch1 Freq
60.02 Hz
Ch1 2.00 V Ch2 2.00 V M 10.0ms A Ch1 1.96 V
0.00000 s
29 Jun 2005
16:48:59

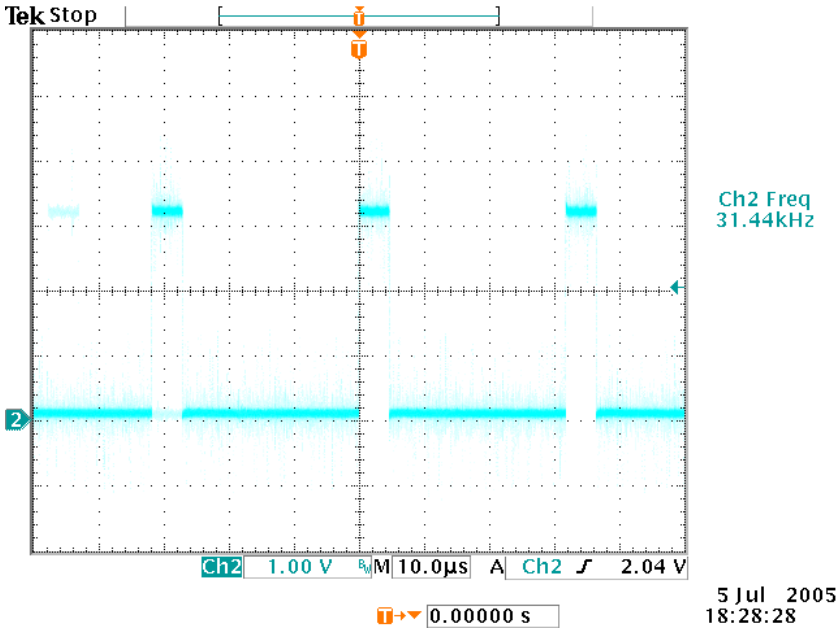

Tek Stop
Ch1 Freq
----.Hz
No period
found
Ch1 2.00 V Ch2 2.00 V M 40.0µs A Ch1 1.96 V
-880.000ns
29 Jun 2005
16:49:32

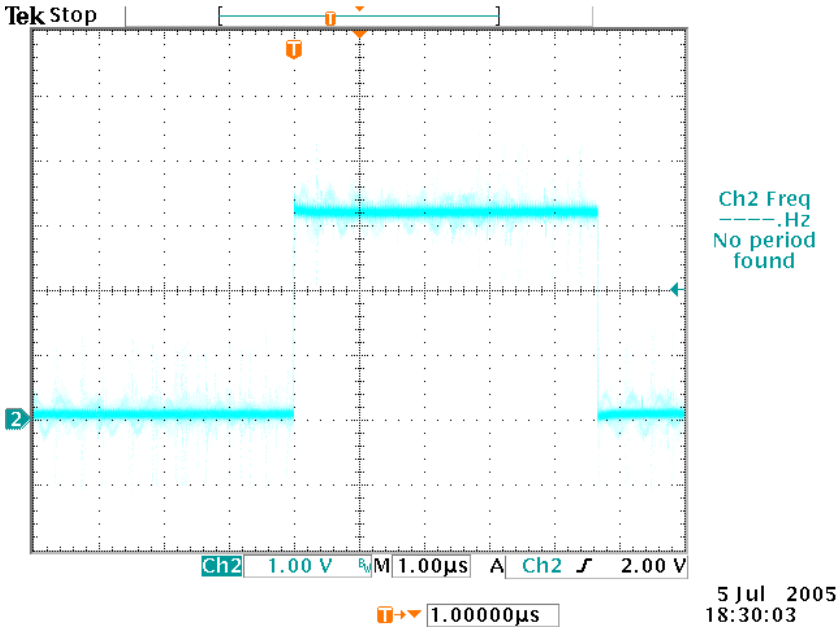
(2) Sil9011CLU (U35 and U42)

CLK

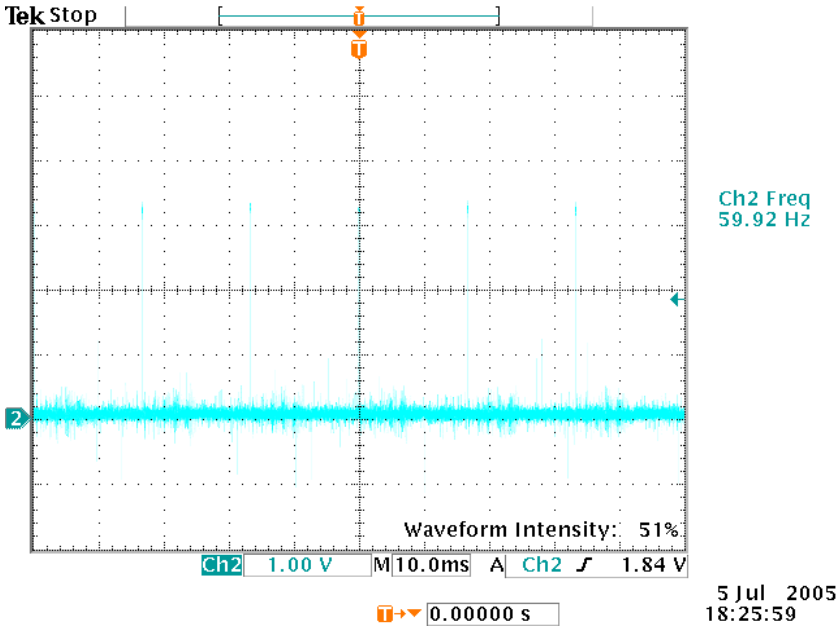


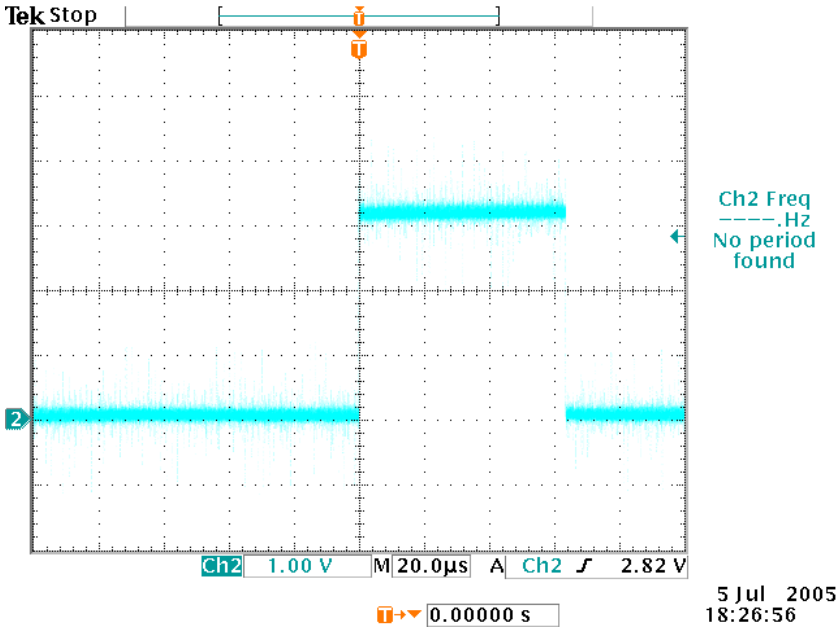
BHS-sync




Tek Stop
Ch2 Freq
----.Hz
No period
found
Ch2 1.00 V M 1.00µs A Ch2 2.00 V
1.00000µs
5 Jul 2005
18:30:03

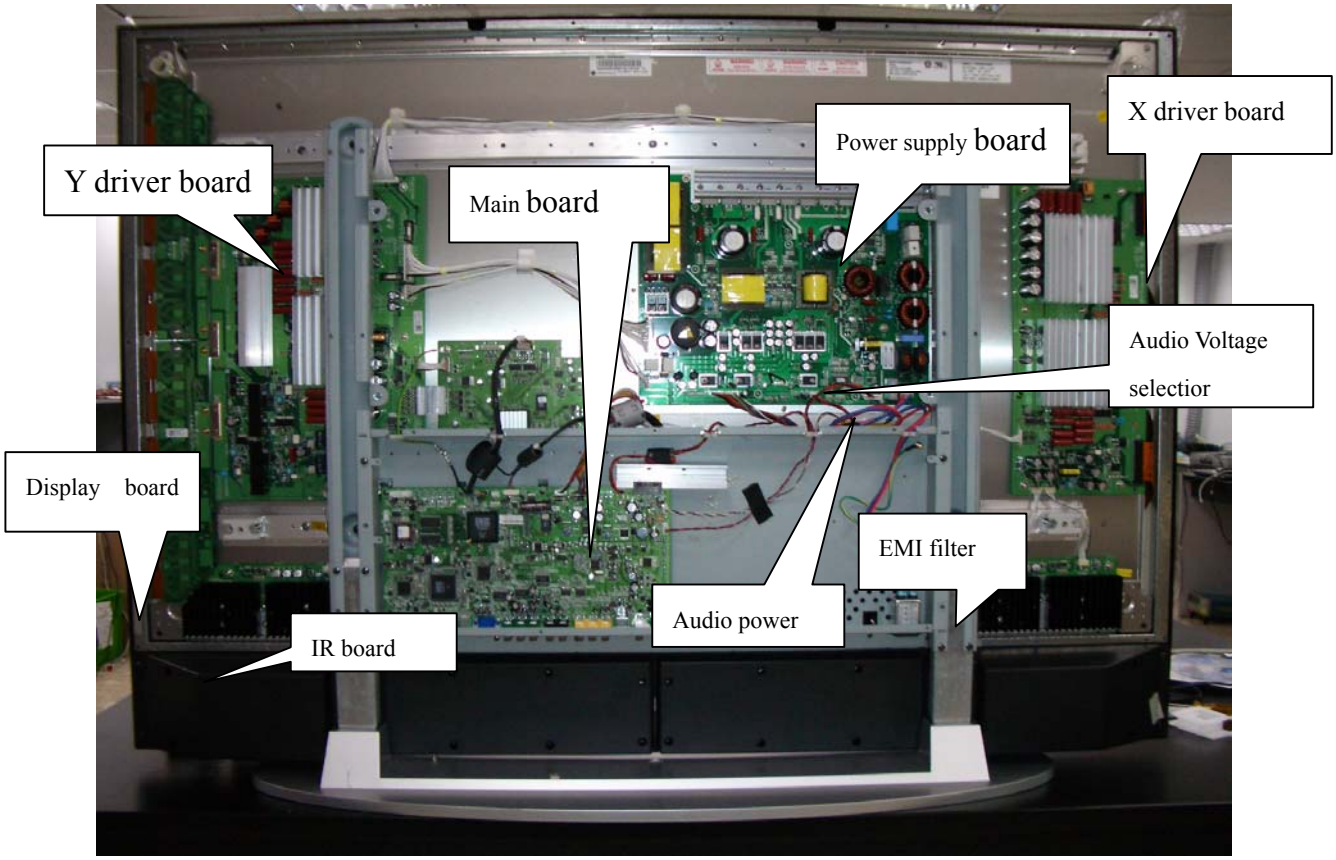
BVS-sync


Tek Stop
Ch2 Freq
59.92 Hz
Waveform Intensity: 51%
Ch2 1.00 V M 10.0ms A Ch2 1.84 V
0.00000 s
5 Jul 2005
18:25:59


Tek Stop
Ch2 Freq
----.Hz
No period
found
Ch2 1.00 V M 20.0µs A Ch2 ƒ 2.82 V
0.00000 s
5 Jul 2005
18:26:56

Chapter 10 PDP Trouble Shooting

A. SYSTEM OVERVIEW

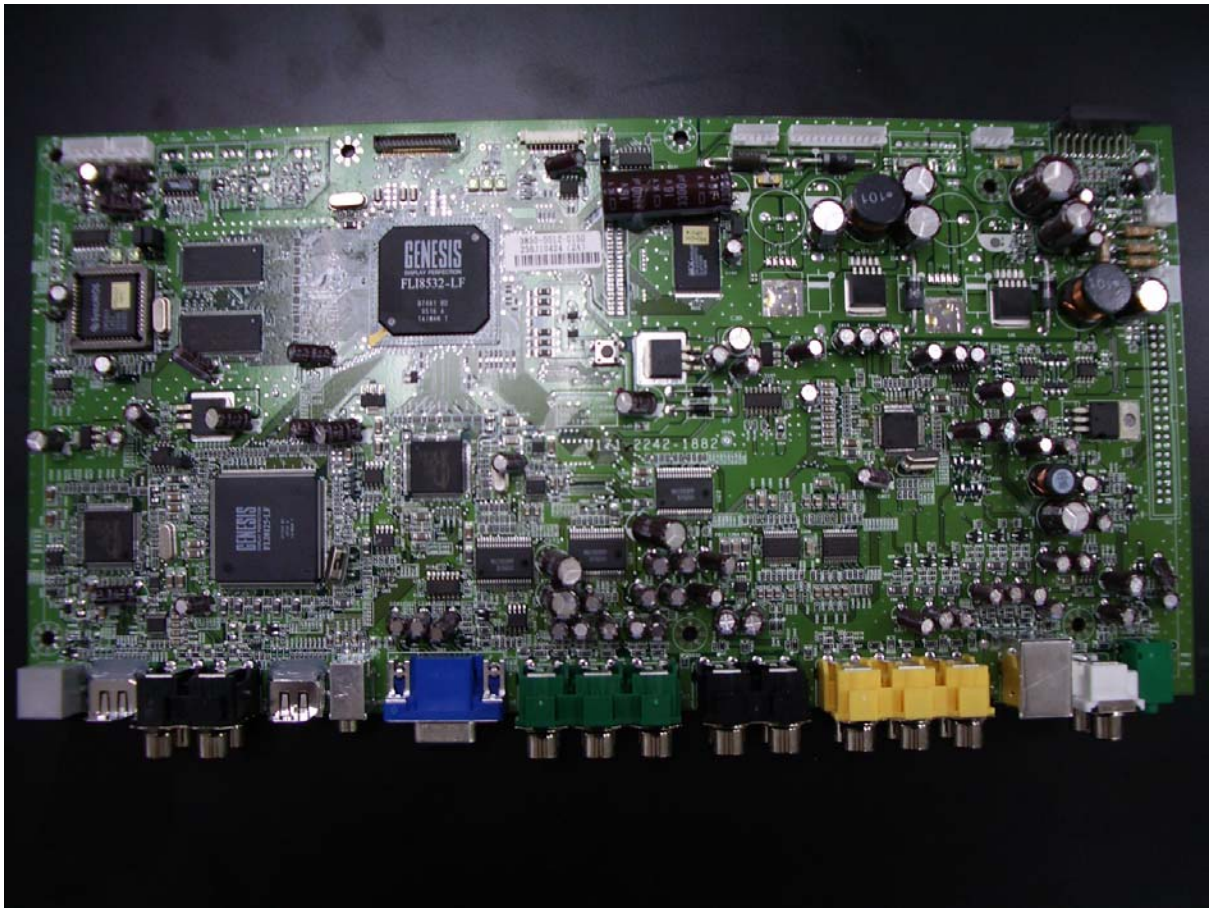


B. PCB PARTS NAME/NUMBER AND FUNCTION DESCRIPTION

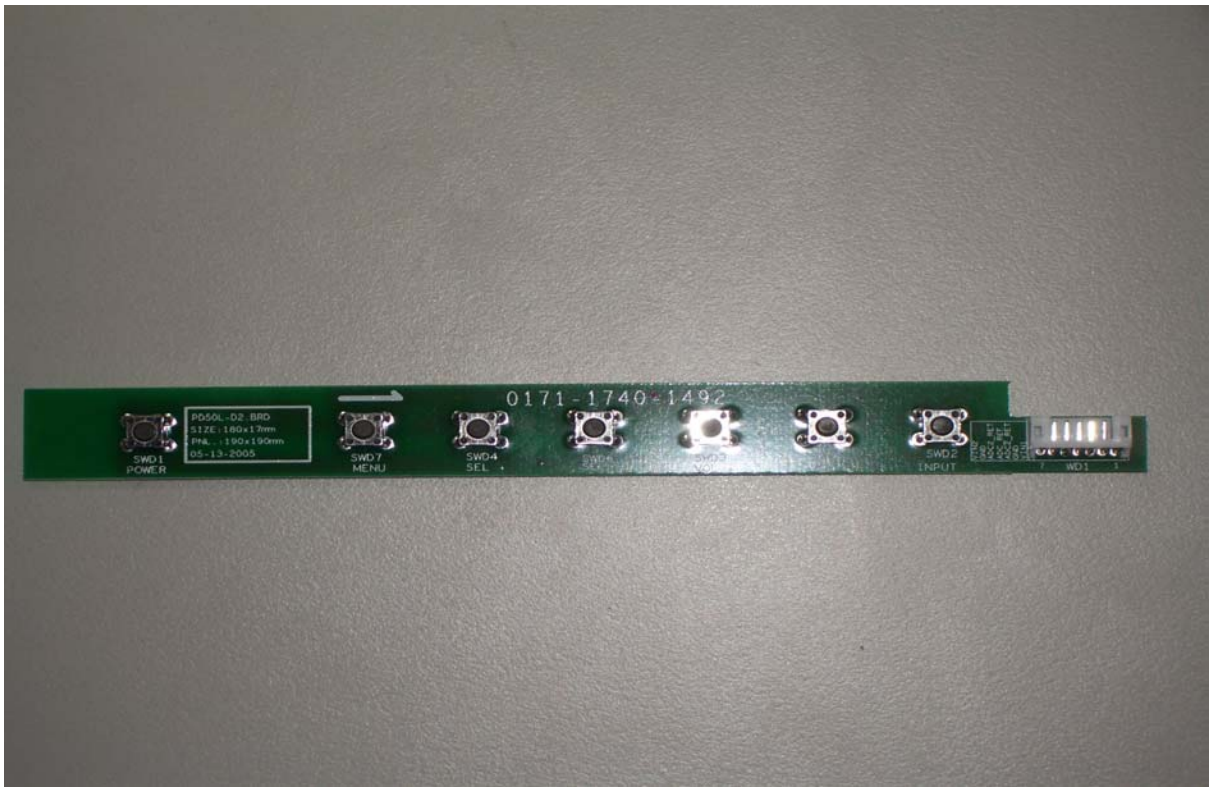
PART NAME	PART NUMBER	FUNCTION DESCRIPTION
POWER SUPPLY BOARD		PROVIDE ALL THE POWER FOR TV SET
X DRIVER BOARD		X ELECTRODE DRIVING BOARD
Y DRIVER BOARD		Y ELECTRODE DRIVING BOARD
AUDIO POWER SELECTOR		AUDIO POWER SUPPLY(+30V OR +24V)
MAIN BOARD	385000120150	CONNECTING TO TRANSFER DISPLY SIGNAL TO PDP SET, AMPLIFIER THE AUDIO SIGNAL TO THE SPEAKER
IR BOARD	385000120189	RECEIVE THE REMOTE CONTROLER AND DISPLAY SYSTEM STATUS LED
DISPLAY BOARD	385000120156	KEYPAD FUNCTION FOR MANUAL OPERATE TV

C. BOARD PICTURE

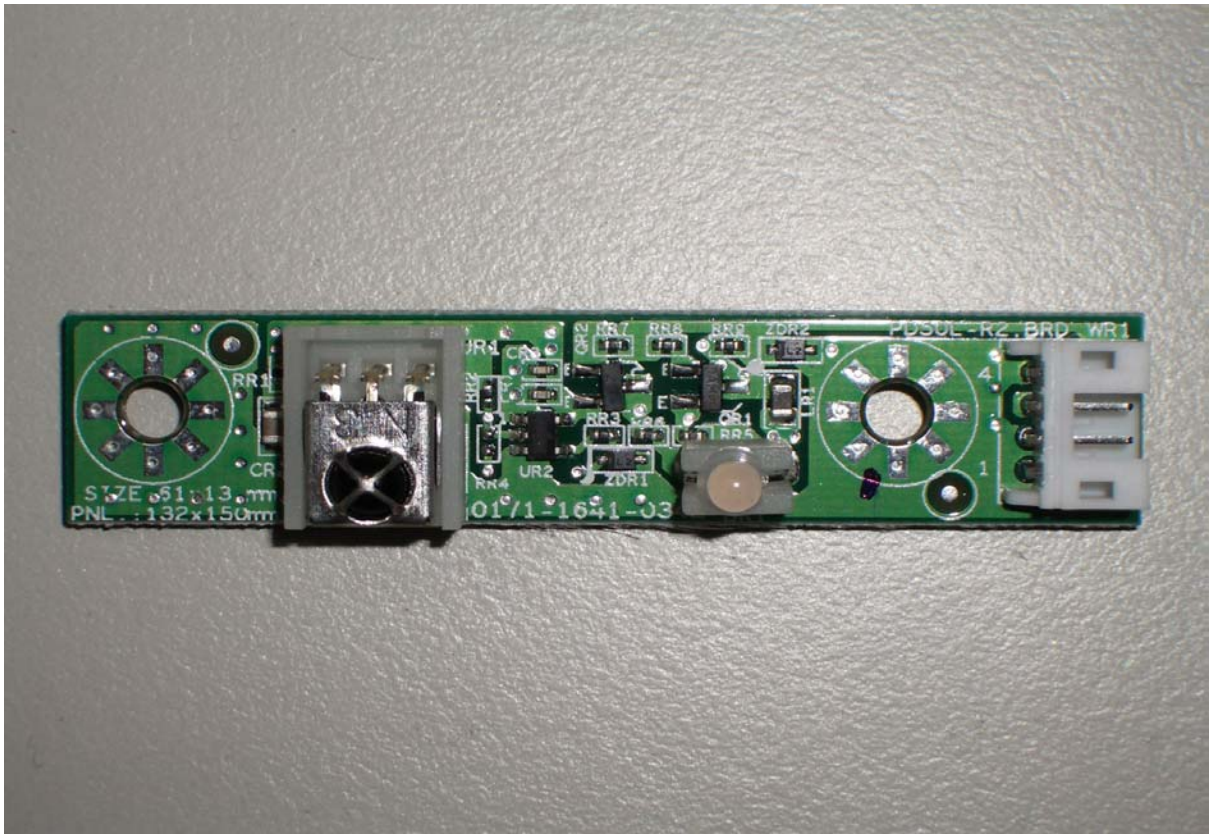
MAIN BOARD



DISPLAY BOARD

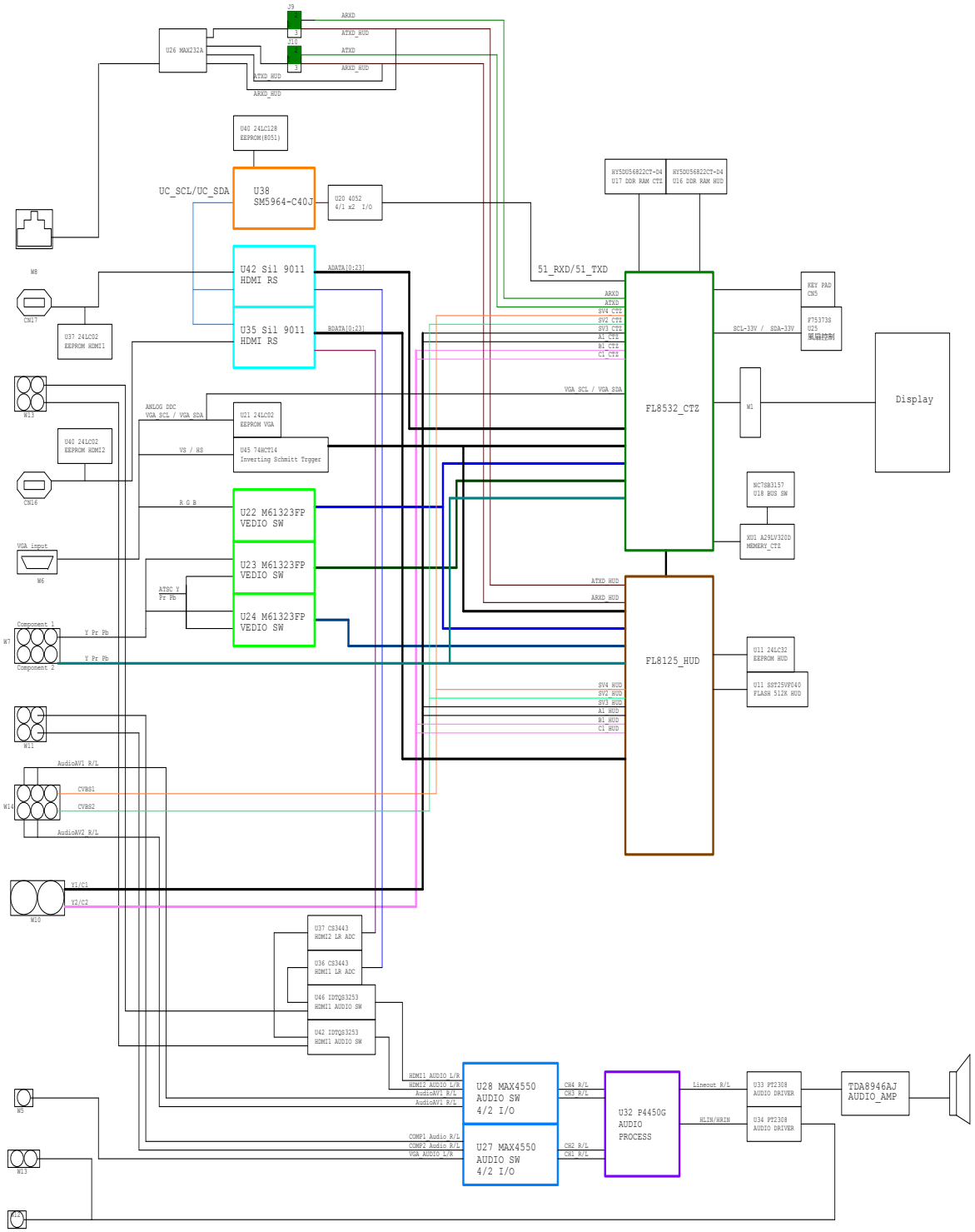


IR BOARD

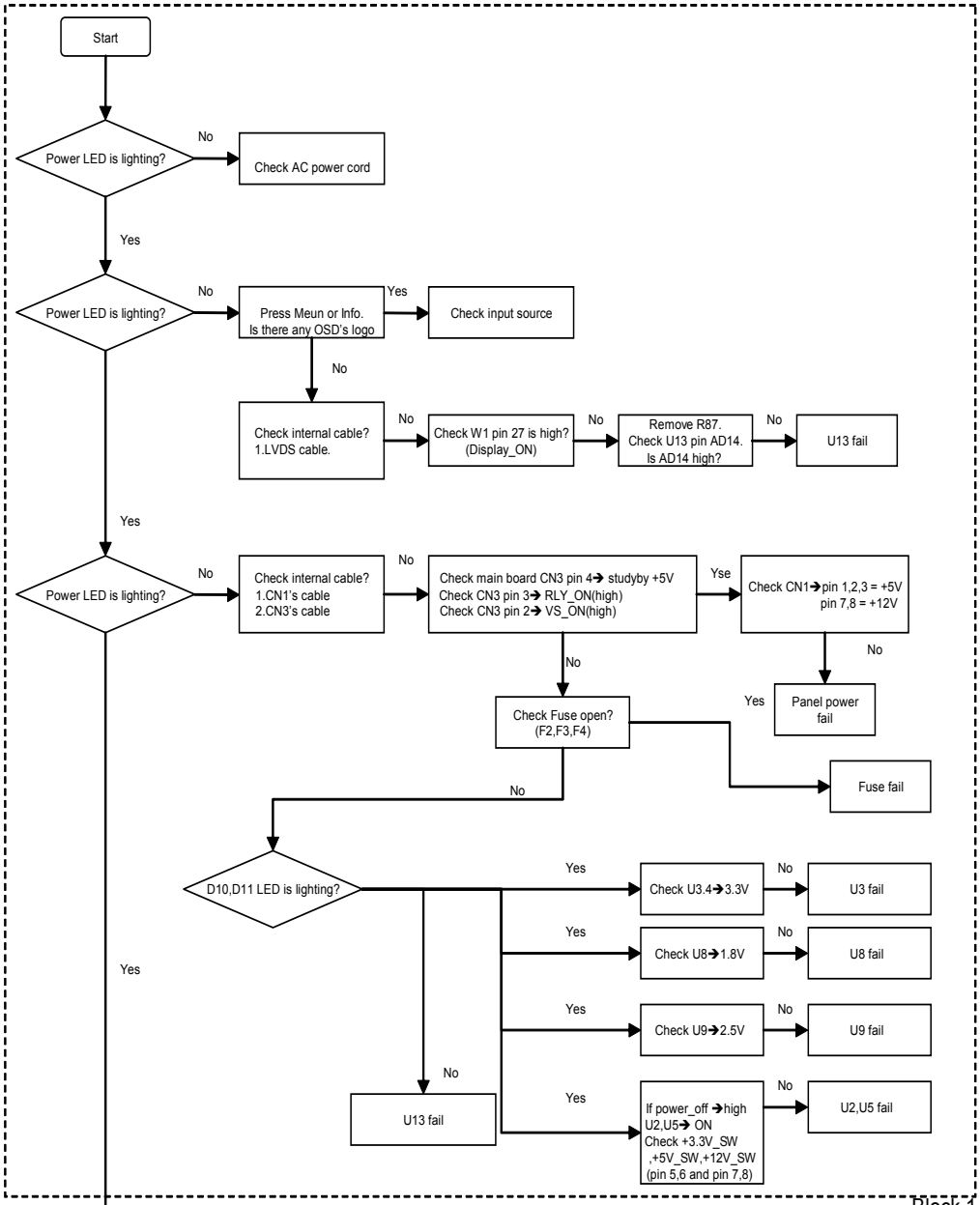


PDP DISPLAY NOTHING

1. Main board block diagram

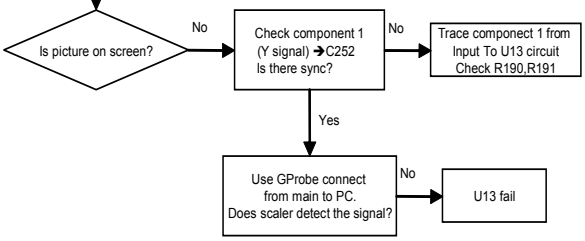


PDP DISPLAY NOTHING(Analog HD1/AC on/off default)



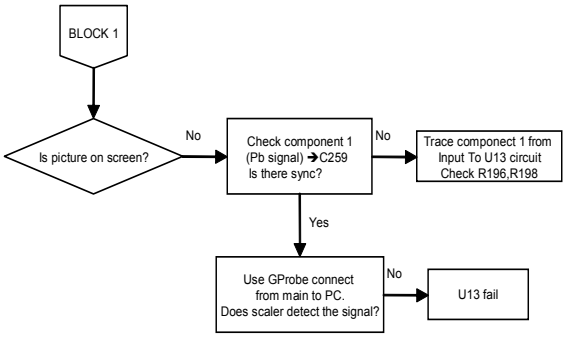
Block 1

PDP DISPLAY NOTHING(Analog HD1 without Y signal)

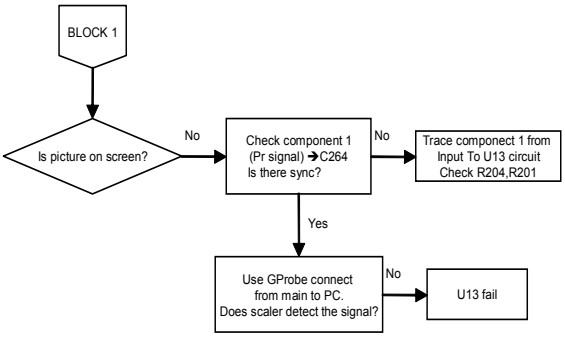


1

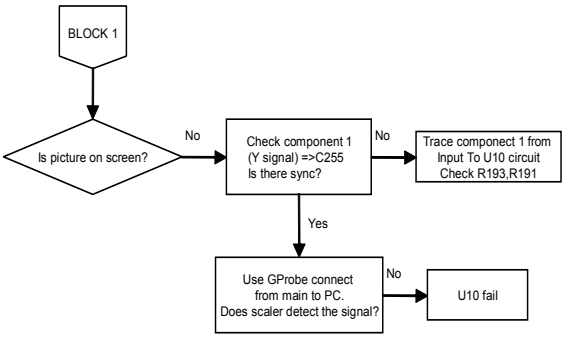
PDP DISPLAY NOTHING(Analog HD1 without Pb signal)



PDP DISPLAY NOTHING(Analog HD1 without Pr signal)

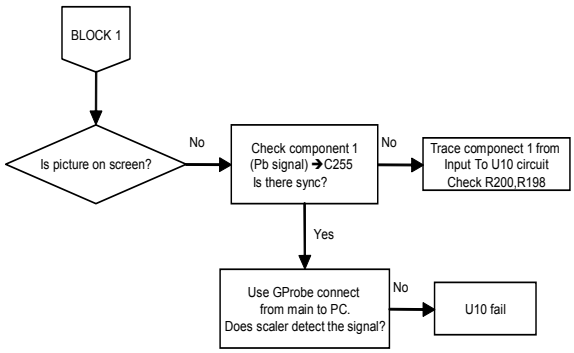


PDP DISPLAY NOTHING(Analog HD1 on PIP mode without Y signal)

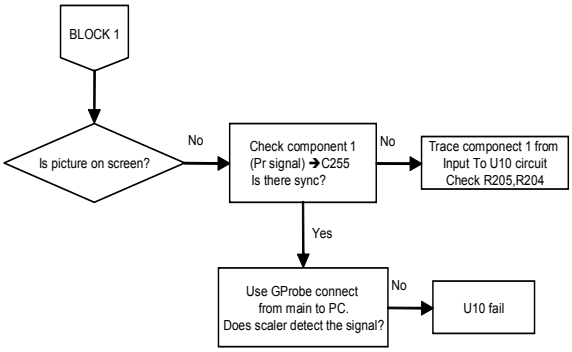


2

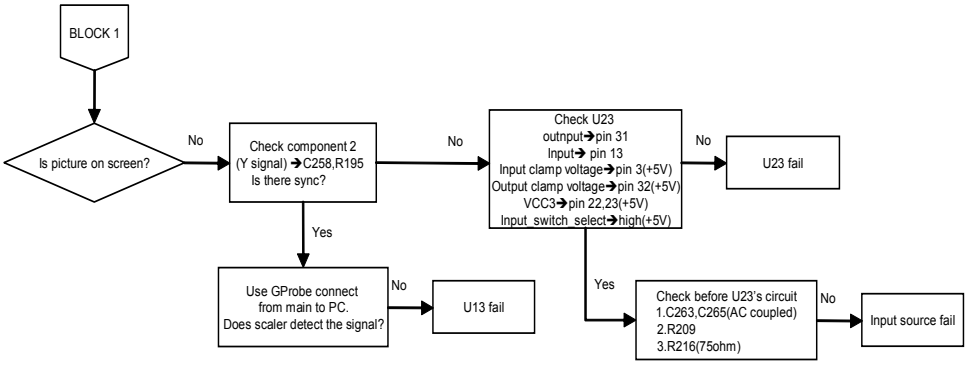
PDP DISPLAY NOTHING(Analog HD1 on PIP mode without Pb signal)



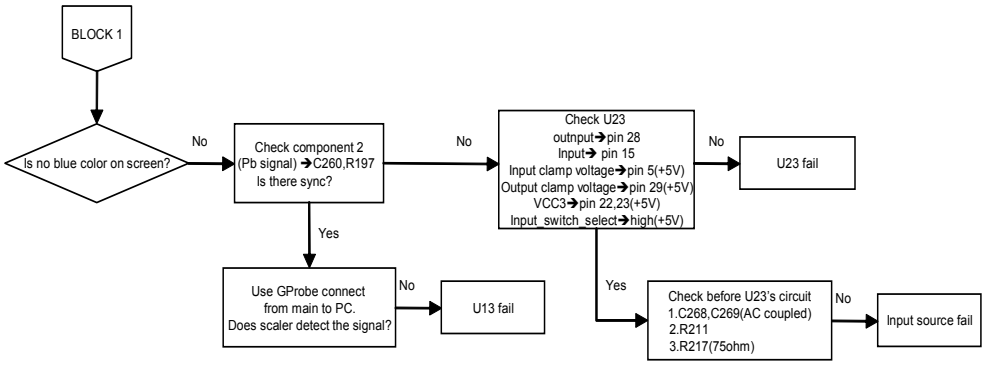
PDP DISPLAY NOTHING(Analog HD1 on PIP mode without Pr signal)



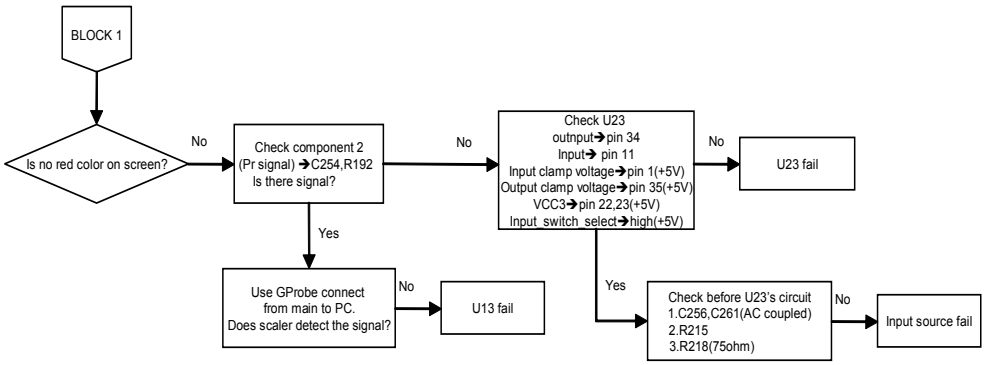
PDP DISPLAY NOTHING(Analog HD2 without Y signal)



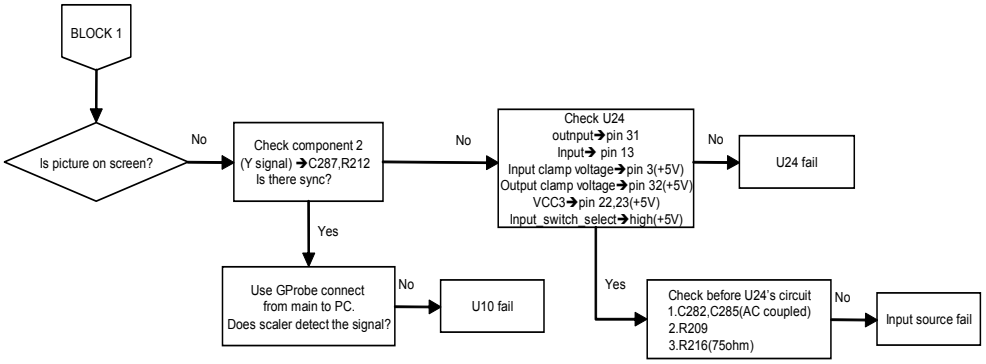
PDP DISPLAY NOTHING(Analog HD2 without Pb signal)



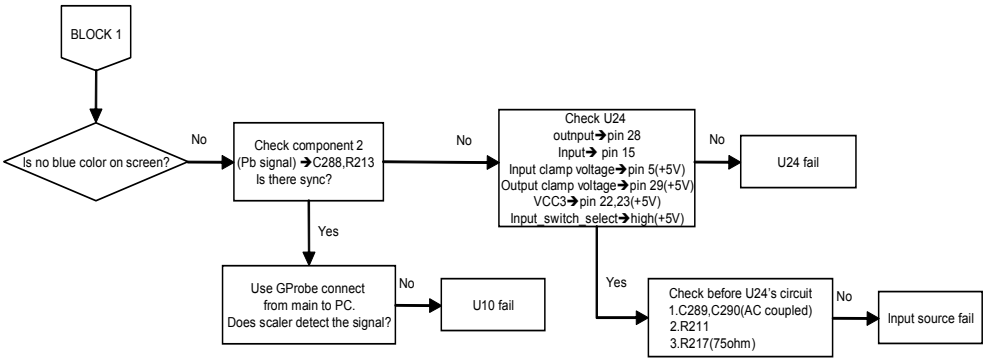
PDP DISPLAY NOTHING(Analog HD2 without Pr signal)



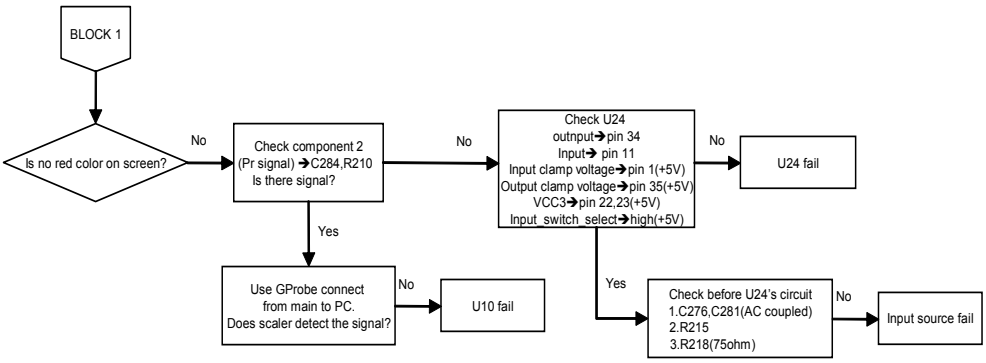
PDP DISPLAY NOTHING(Analog HD2 on PIP mode without Y signal)



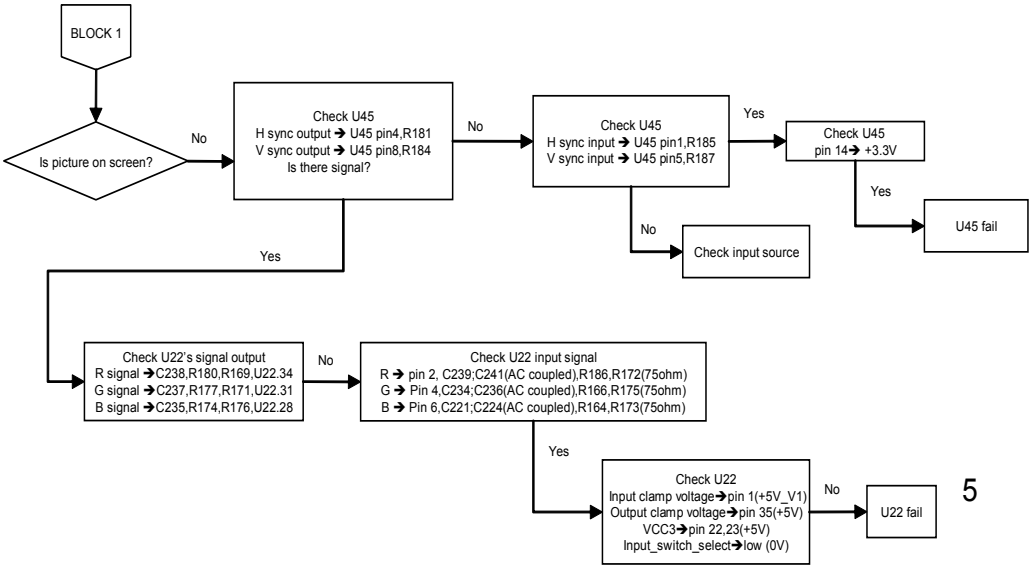
PDP DISPLAY NOTHING(Analog HD2 on PIP mode without Pb signal)



PDP DISPLAY NOTHING(Analog HD2 on PIP mode without Pr signal)

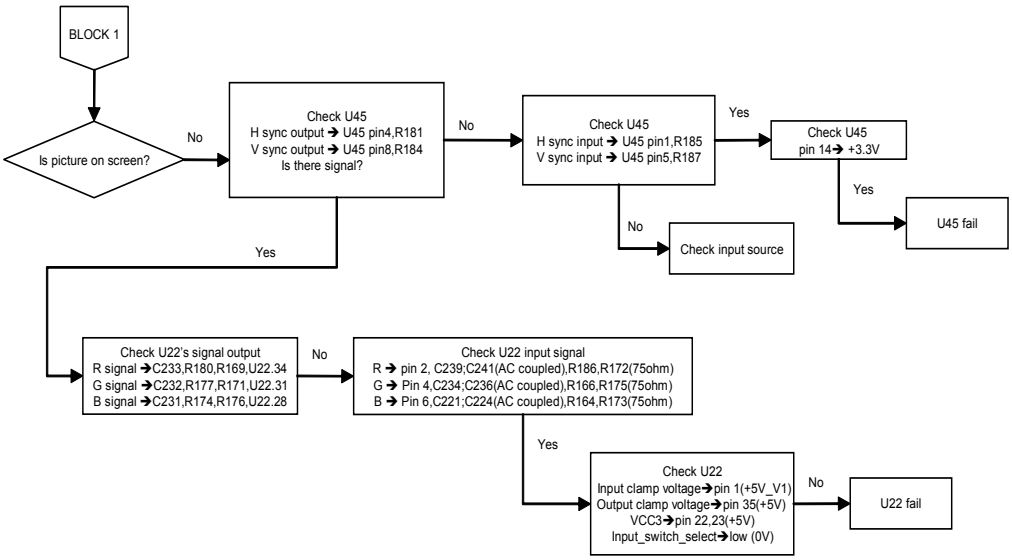


PDP DISPLAY NOTHING(RGB)

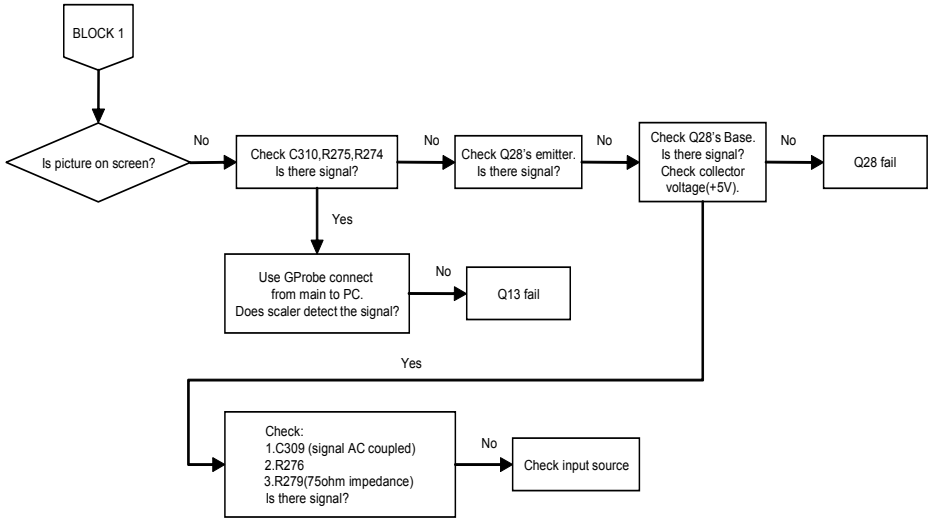


5

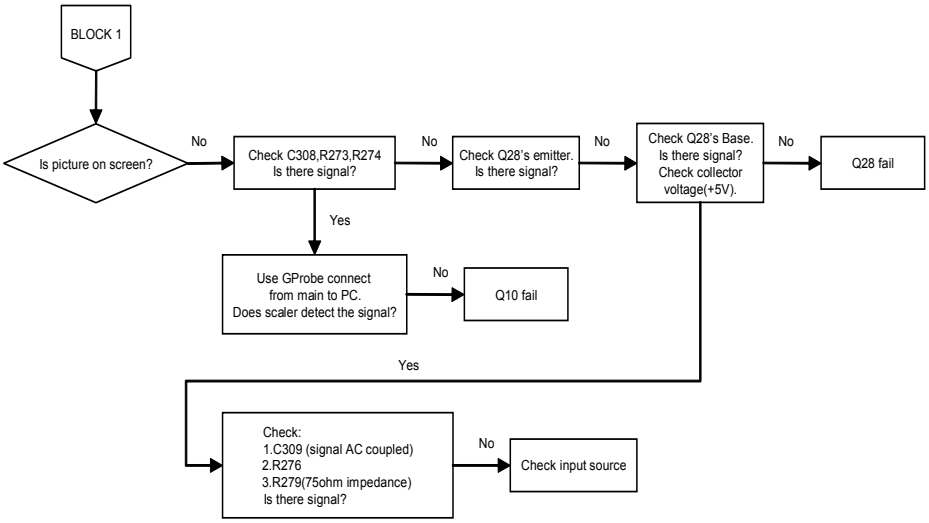
PDP DISPLAY NOTHING(RGB on PIP mode without screen)



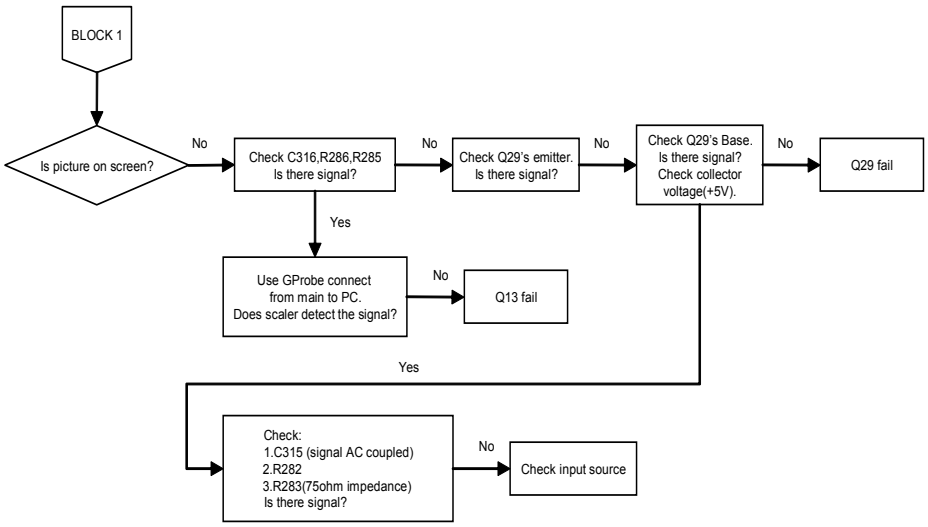
PDP DISPLAY NOTHING(Composite 1 without screen)



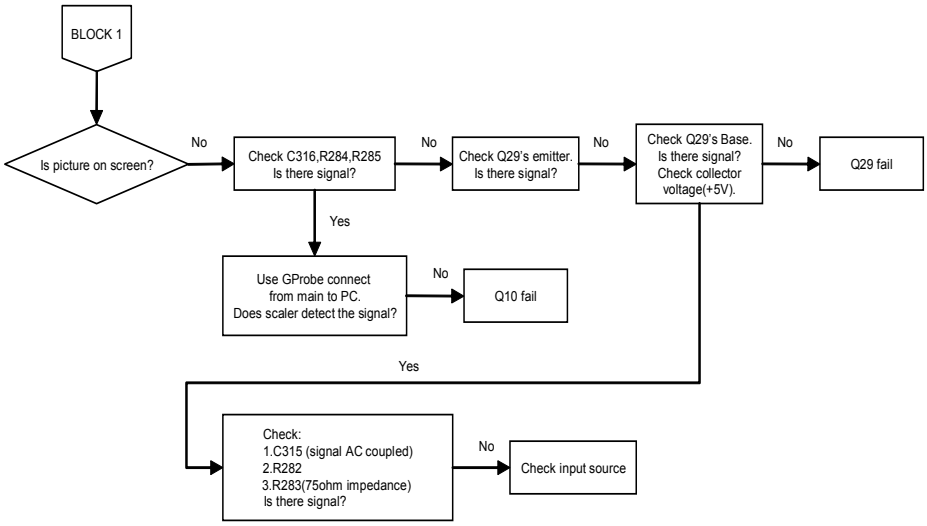
PDP DISPLAY NOTHING(Composite 1 on PIP without screen)



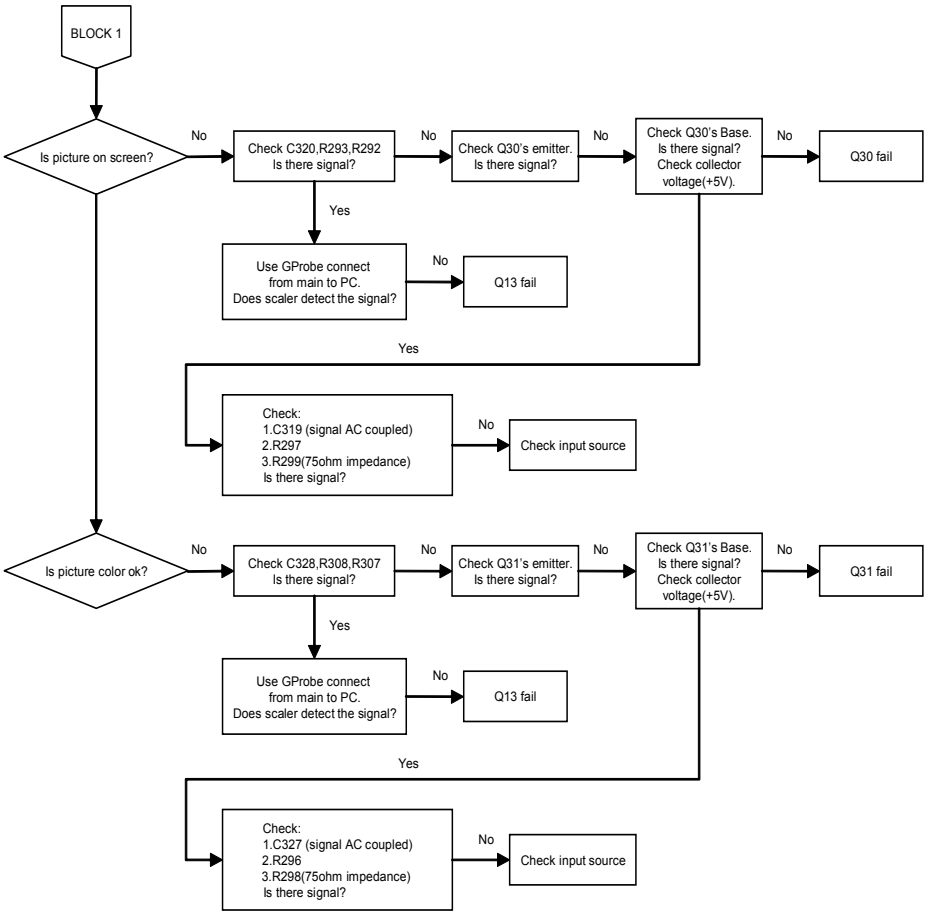
PDP DISPLAY NOTHING(Composite 2 without screen)



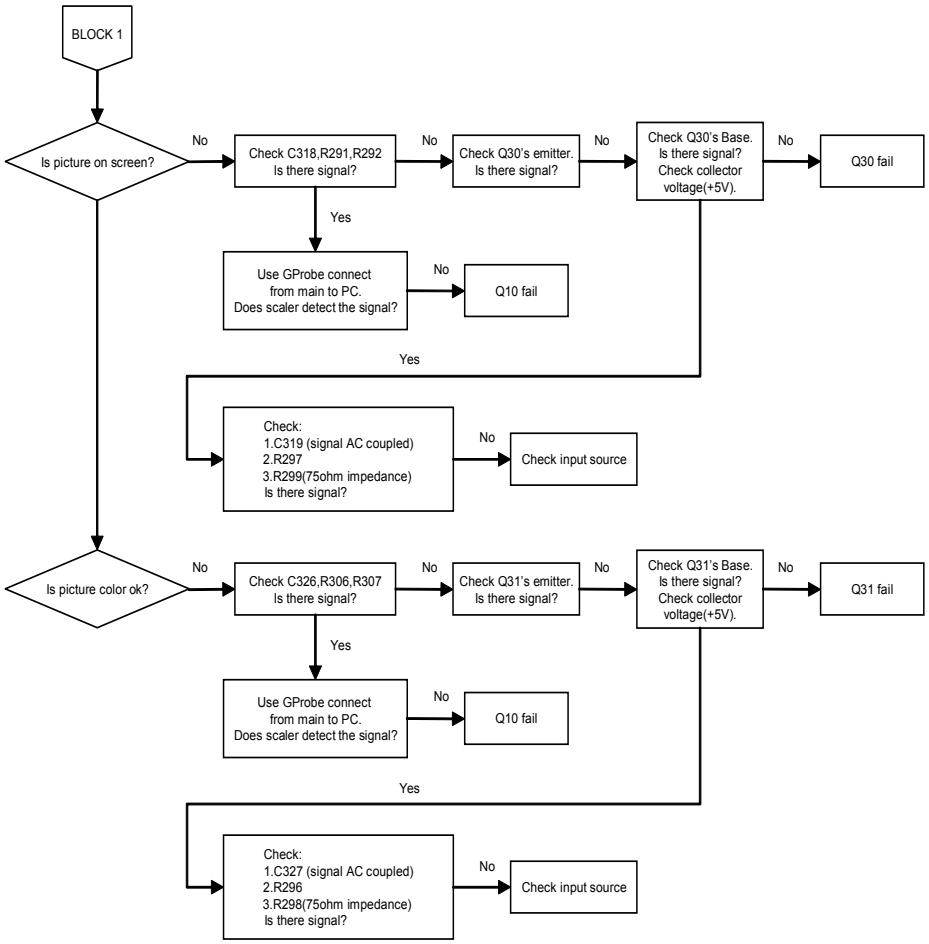
PDP DISPLAY NOTHING(Composite 2 on PIP without screen)



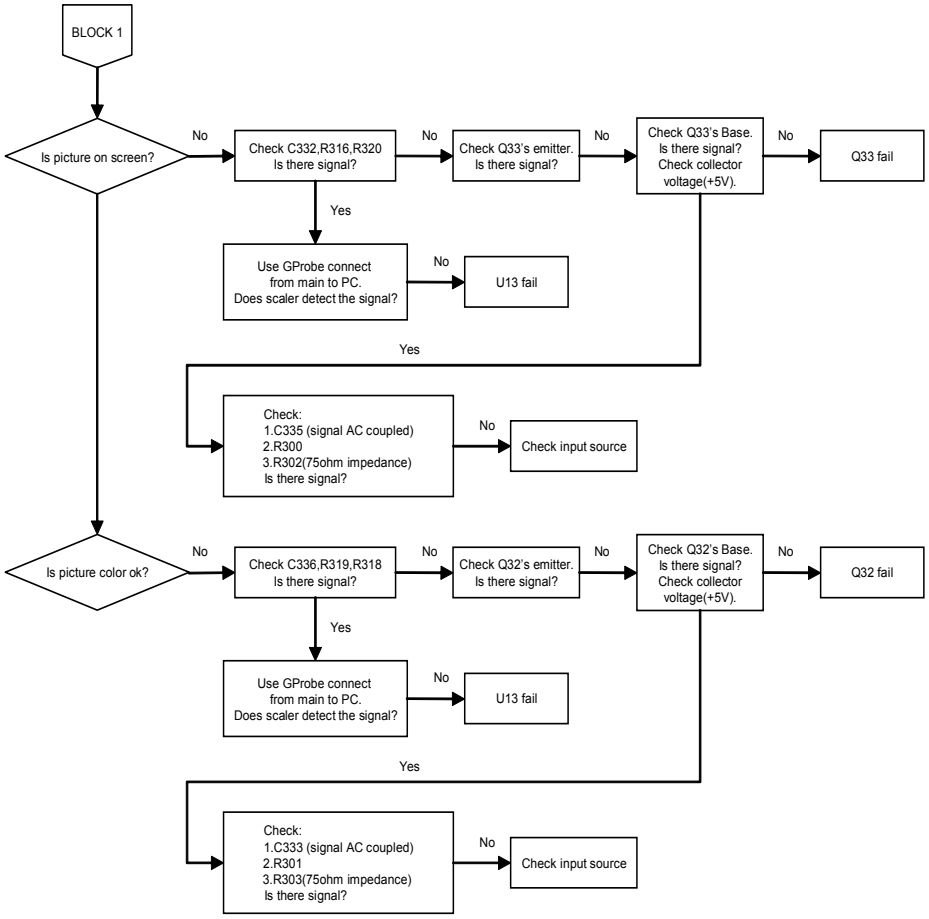
PDP DISPLAY NOTHING(S-VIDEO 1 without screen)



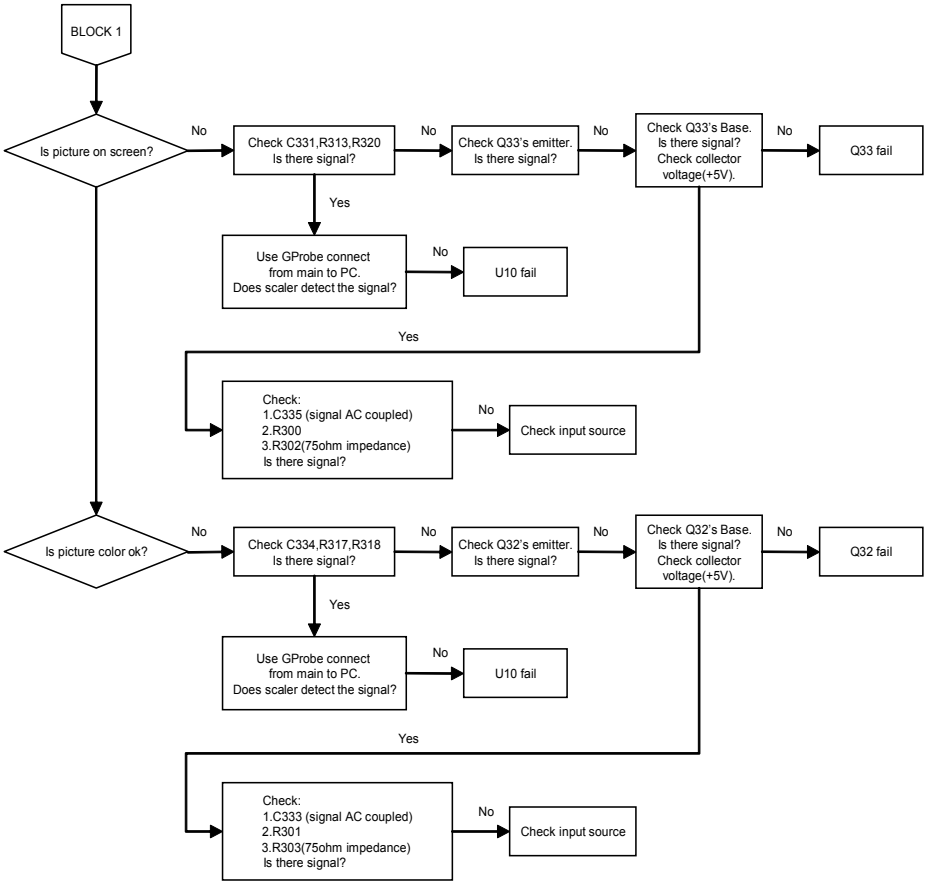
PDP DISPLAY NOTHING(S-VIDEO 1 on PIP mode without screen)



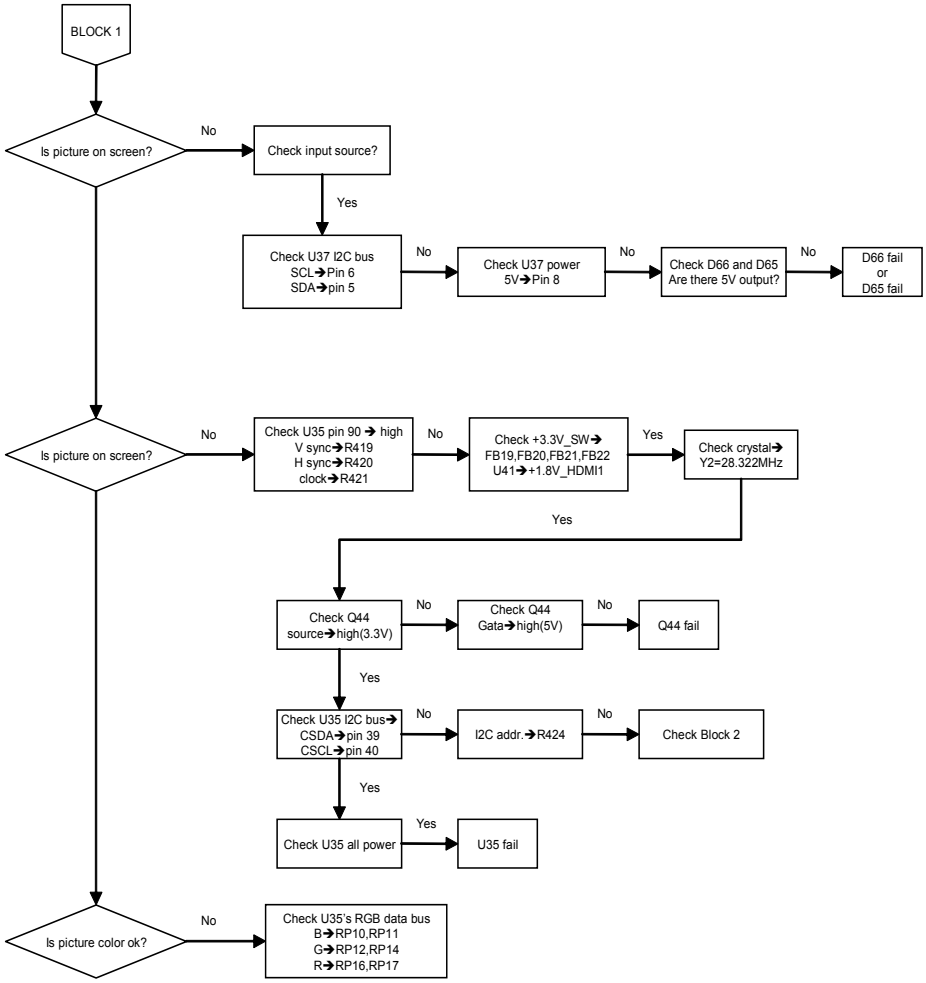
PDP DISPLAY NOTHING(S-VIDEO 2 without screen)



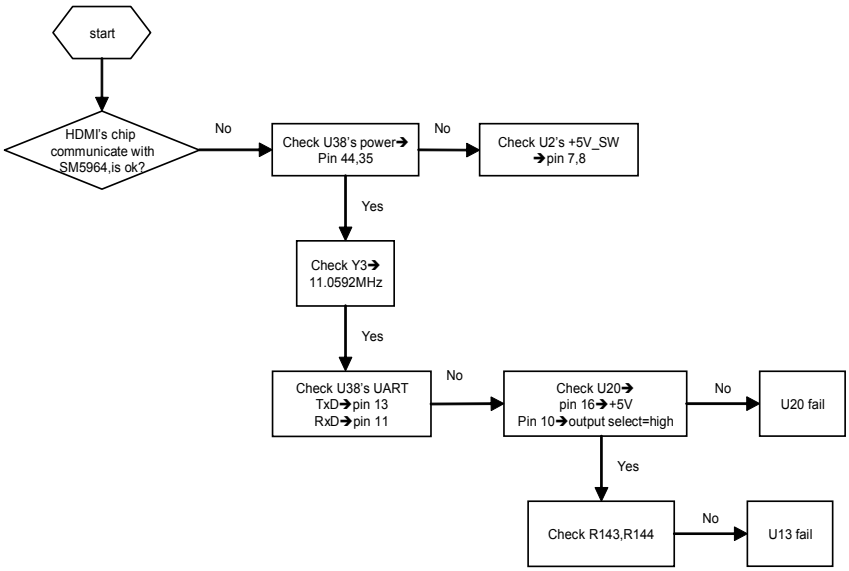
PDP DISPLAY NOTHING(S-VIDEO 2 on PIP mode without screen)



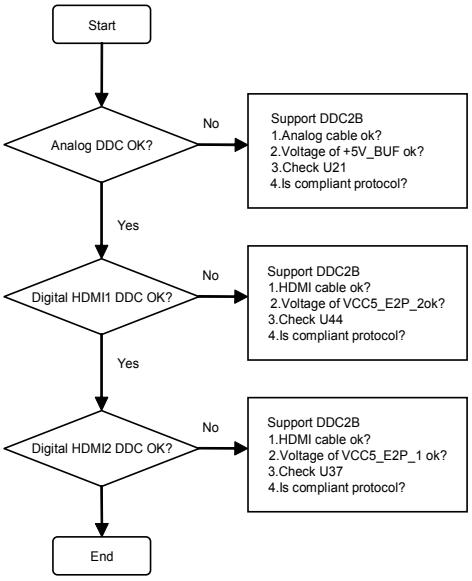
PDP DISPLAY NOTHING(Digital 2 U35 with PORT B without screen)



Block 2


start
HDMI's chip communicate with SM5964,is ok?
No
Check U38's power→ Pin 44,35
No
Check U2's +5V_SW →pin 7,8
Yes
Check Y3→ 11.0592MHz
Yes
Check U38's UART TxD→pin 13 RxD→pin 11
No
Check U20→ pin 16→+5V Pin 10→output select=high
No
U20 fail
Yes
Check R143,R144
No
U13 fail

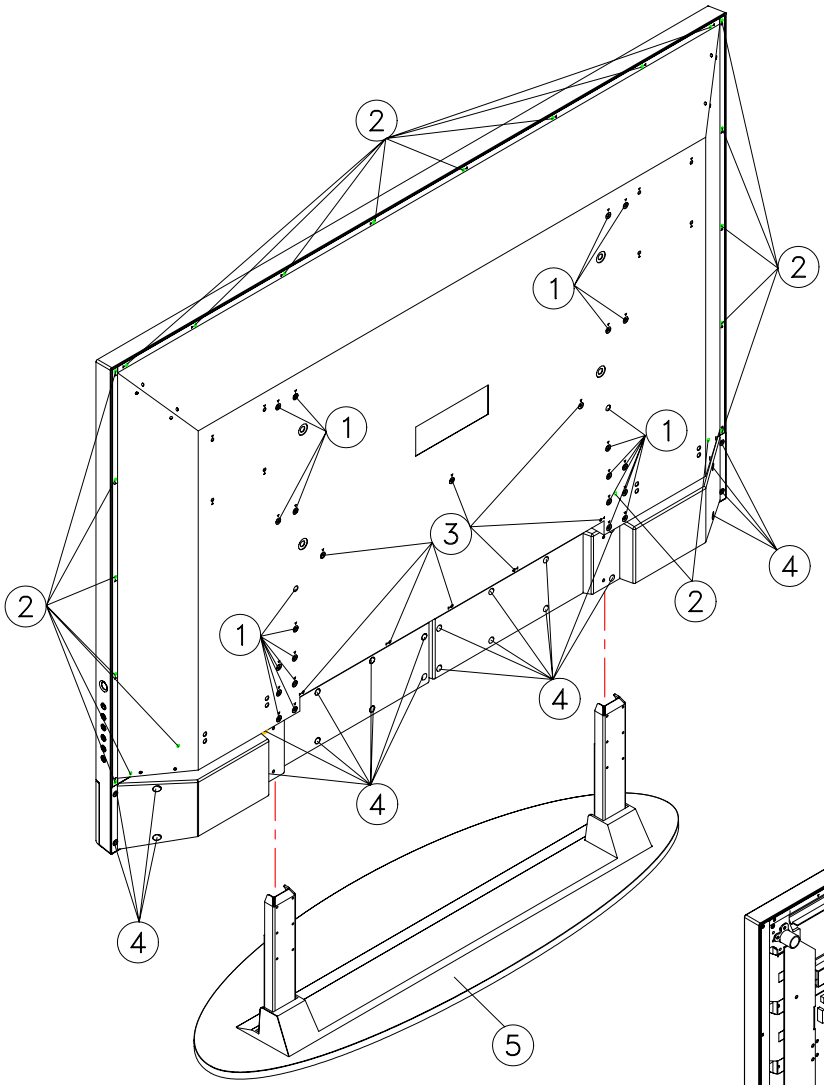
TROUBLE OF DDC READING

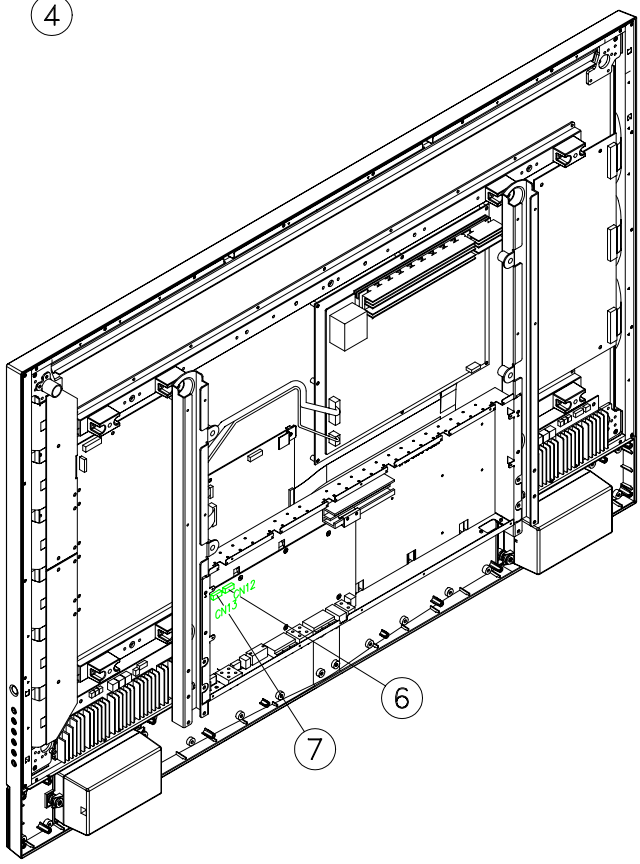


1.REAR COVER ASS'Y REMOVAL

Note:Spread a mat underneath to avoid damaging the Plasma surface.

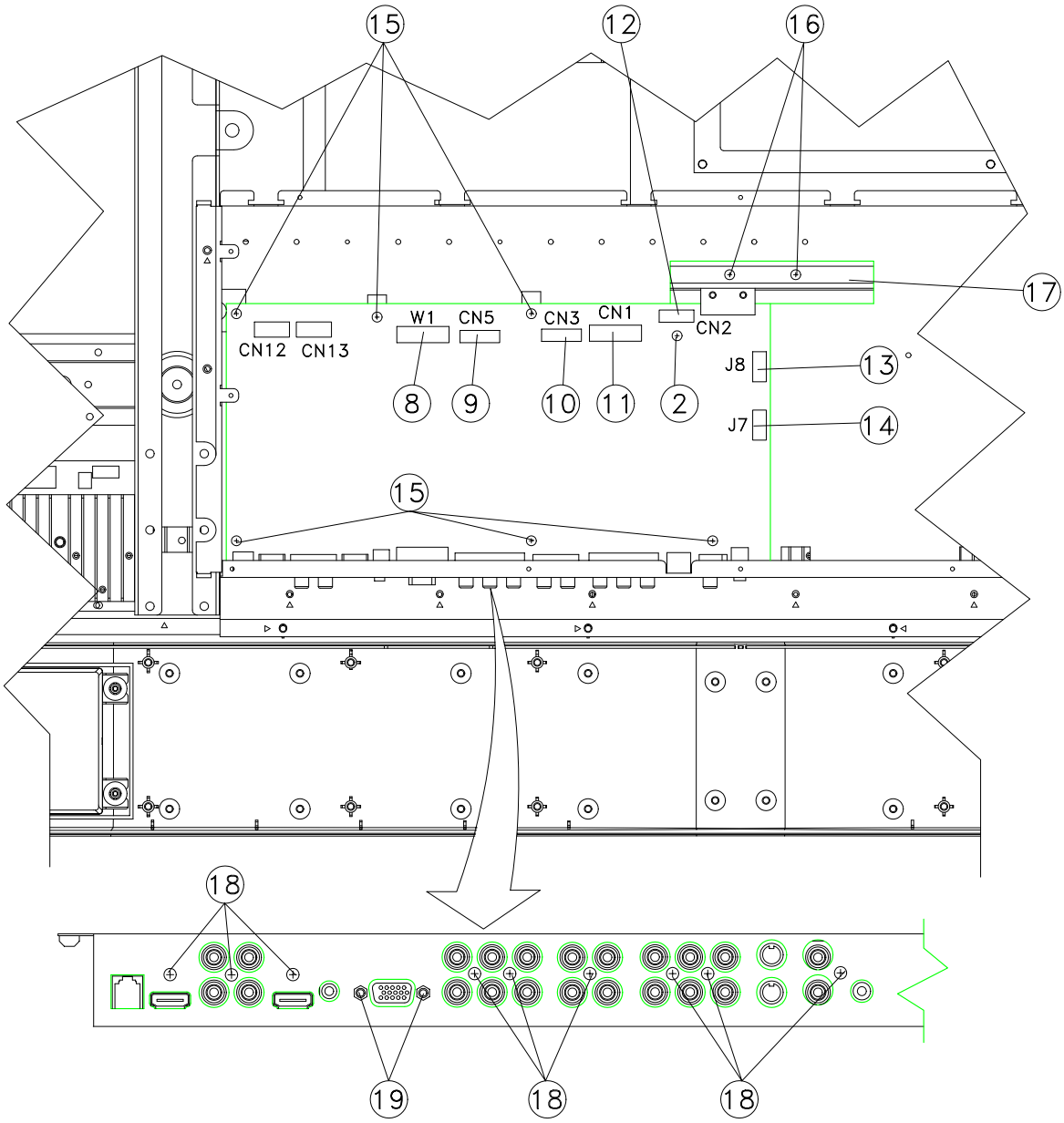
1) Remove twenty-four screws ① from rear cover.
2) Separate the Bass Ass'y ⑤ .
3) Remove twenty-two screws ② and eight screws ③ from rear cover.
4) Remove the connector ⑥ (CN12) ⑦ (CN13) of the Fan cable.
5) Separate the rear cover.
6) Remove twenty-four screws ④ from speaker rear cover right / left .
7) Separate the speaker rear cover right / left.



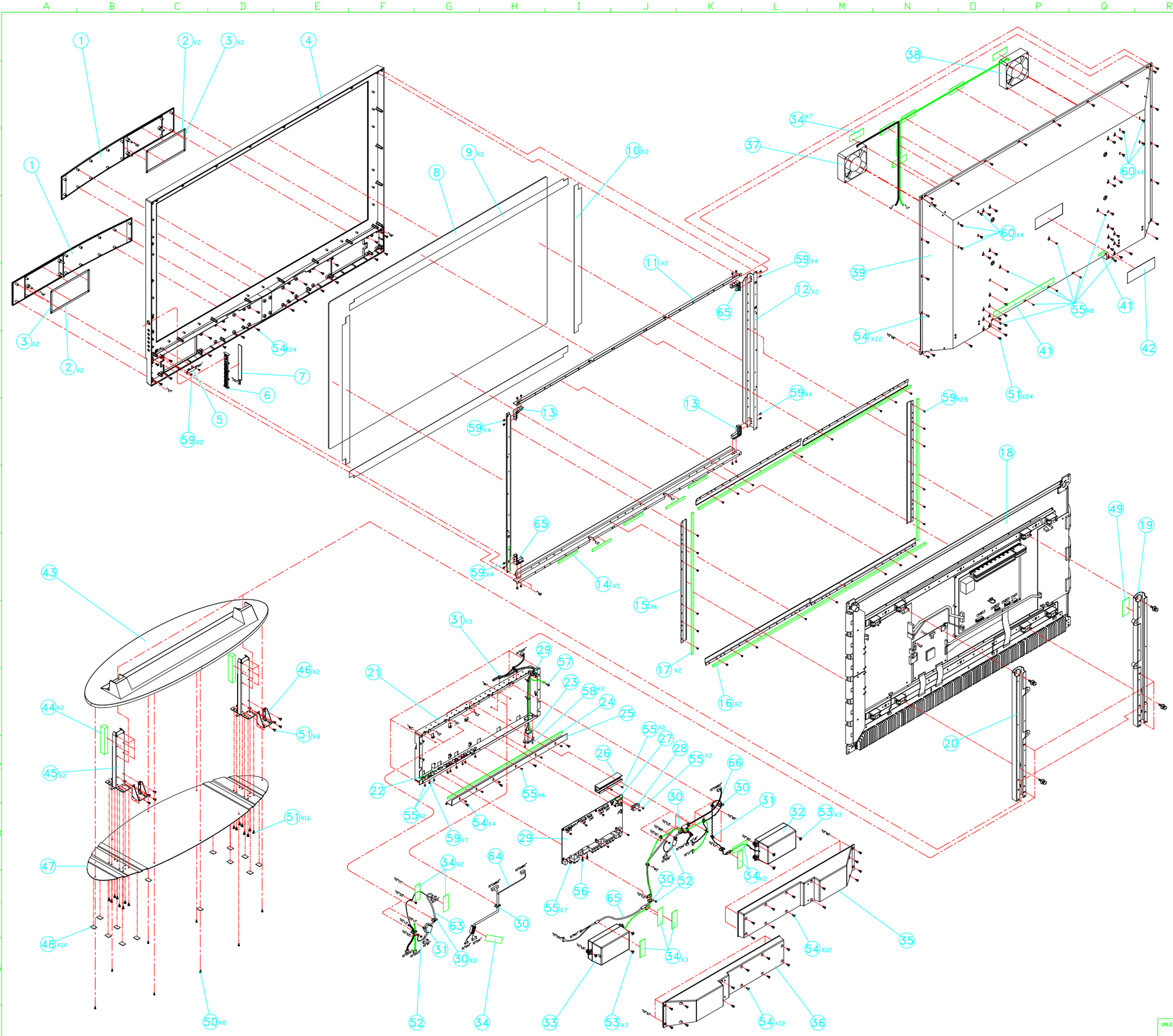


2. MAIN BD ASS'Y REMOVAL

1) Remove the connector ⑧(W1) of the Main bd cable1.
2) Remove the connector ⑨(CN5) of the keypad +IR cable.
3) Remove the connector ⑪(CN1) ⑩ (CN3) of the Main bd cable 2.
4) Remove the connector ⑫(CN2) of the Main bd cable 3.
5) Remove the connector ⑬(J8) ⑭(J7) of the speaker cable.
6) Remove the seven screws ⑮ from Main bd Ass'y.
7) Remove two screws ⑯ from heaksnik ⑰.
8) Remove nine screws ⑱ and two hexagon ⑲ from PCB support .
9) Separate the Main BD Ass'y.



D:/VIZIO-P50HDM-REMOVAL.DWG



ITEM	PART NO.	DESCRIPTION	QTY
1	1701-1923-4010	SPEAKER NET(PD-50L)	1
2	1947-1400-0160	NON-WOVEN-FABRICS(200L*7W*0.5H)	4
3	1947-1400-0150	NON-WOVEN-FABRICS(200L*7W*0.5H)	4
4	1801-0119-6010	FRONT BEZEL VIZIO P50HDM(PMMA.BLACK)ASS'Y	1
5	3850-0012-0189	PDP IR BD ASS'Y(PD-50L)	1
6	1701-0416-0010	BUTTON(PD-50LM)(PMMA)	1
7	3850-0012-0156	PDP DISPLAY BD ASS'Y(PD-50L)	1
8	1701-0900-1610	PDP FILTER 50" 5X10(FG501PAA-01)(LG)	1
9	1947-1800-0820	CONDUCTIVE FABRIC TAPE(40W*1162.6L)mm	2
10	1947-1800-0810	CONDUCTIVE FABRIC TAPE(40W*678.6L)mm	2
11	1712-0100-8270	FILTER BRACKET TOP(PD-50LM)	2
12	1712-0100-8290	FILTER BRACKET RIGHT(PD-50LM)(SECC T+0.8mm)	2
13	1701-0800-0980	BKT-SUPPORTOR-TR-BL(PD-50LM)(PC)	2
14	1947-1800-0790	GASKET BLOCK(100L*10.W*1.0H)mm	6
15	1712-0500-1570	FILTER CLIP(SPTE=0.3mm)(PD-50LM)	6
16	1947-1500-2340	PANEL CUSHION-H(LENGTH=1130mm)(pd-50lm)	2
17	1947-1500-2350	PANEL CUSHION-V(LENGTH=650mm)(PD-50LM)	2
18	0213-0500-0261	PDP MODULE 50" PDP50X3(LG)	1
19	1712-0100-8230	MAIN FRAME RIGHT(PD-50LM)()SECC T=0.8mm)	1
20	1712-0100-8240	MAIN FRAME LEFT(PD-50LM)(SECC T=0.8mm)	1
21	1712-0100-8320	PCB SUPPORT(PD-50LM)(SECC T=0.8mm)	1
22	1947-1800-0880	GASKET BLOCK(9W*1H*70L)	1
23	0320-4000-0142	POWER CORD 110V UL/CSA 1800mm BLK N. M.	1
24	1947-1800-0870	GASKET BLOCK(610L*8W*2H)mm	1
25	1712-0100-8260	I/O BRACKET (PD-50LM)(SECC T=0.8mm.black)	1
26	1712-0400-0720	HEAK SINK(PD-42S)	1
27	1947-1900-0030	HEATPATH(25X14mm)	1
28	1712-0100-4590	HEAT SINK FIX MTEAL(TM-30A)	1
29	3850-0012-0150	PDP MAIN BD ASS'Y(PD-50L)	1
30	1701-1500-1080	EDGE ASDDLE DS-12(NYLON)	8
31	1701-1500-0450	WIRE SADDLR(CH-01B)	16
32	0335-0008-0351	SPEAKER 8ohm 10W BOX 1045mm CORE*1P302GR	1
33	0335-0008-0451	SPEAKER 8ohm 10W BOX 840mm CORE*1P302GL	1
34	1947-1200-0310	ACETATE CLOTH TAPE(27*75mm)	14
35	1701-1923-5010	SPEAKER REAR COVER RIGHT(PD-50L)	1
36	1701-1923-6010	SPEAKER REAR COVER LEFT(PD-50L)	1
37	0973-1200-1051	FAN 12V1800 rpm 120*120 L=640mm 4P FD121225LB.	1
38	0973-1200-2051	FAN 12V1800 rpm 120*120 L=1150mm FD121225LB	1
39	1712-0100-8250	REAR COVER(PD-50LM)(SECC T=1mm,BLACK)	1
40	1701-0800-1530	REAR PLATE VIZIO P50HDM	1
41	1701-0800-1540	AC IN PLATE VIZIO (P50HDM)	1
42	1936-1100-7780	BACK LBL VIZIO P50HDM	1
43	1701-0519-1010	BASE COVER(PD-50LM)	1
44	1947-1800-0860	GASKET BLOCK(17W*21H*120L)mm	2
45	1712-0100-8310	BASE FRAME(PD-50LM)	2
46	1712-0100-8350	CORNER-SUPPORT(PD-50LM)(SECC T=2mm)	2
47	1712-0100-8340	BASE-PLATE(PD-50LM)(SECC T=2mm)	1
48	1701-1000-0450	FOOT(PORON)(20L*15W*1H)	14
49	1701-0900-1670	MYLAR 72*35*0.4mm	1
50	1721-3003-0820	TAP.SCREW-TF #M3.0*8.0L,Ni	8
51	1720-0004-0850	MAC.SCREW-MB M4.0*8.0L,BLK-Ni	–
52	1720-0103-0520	MAC.SCREW-MBFW M3.0*5.0L.Ni	3
53	1721-4103-0820	TAP.SCREW-TRF #3.0*8.0L,Ni	6
54	1721-0004-1050	TAP.SCREW-TP#4.0*10.0L,BLK-Ni	–
55	1720-0003-0650	MAC. SCREW-MB M3.0*6.0L,BLK-Ni	–
56	1720-7344-0820	MAC.SCREW-MHSW #4-40*8.0L,Ni	2
57	1720-1204-0820	MAC.SCREW-MPGW M4.0*8.0L,Ni	1
58	1720-3003-0850	MAC.SCREW-MF M3.0*8.0L,BLK-Ni	2
59	1721-0003-0620	TAP.SCREW-TB#3.0*6.0L,Ni	–
60	1721-1005-0850	TAP.SCREW-TB #4.7*8L.BLK-Ni	8
61	0460-4131-0011	WH FI-W31S/FI-W31S 20276 230mm CORE*2	1
62	0460-2119-0010	WH PH5P+PH12P-EI7P+EI12P 1007#24 480/330mm	1
63	0460-3010-0111	WH5102110-PH7P+PH4P995/883mm shield core*3	2
64	0460-1004-0320	WH PH4P-EI4P 1007#24 380mm	1
65	1701-0800-0990	BKT-SUPPORTOR-TL-BL(PD-50LM)(PC)	2

VIZIO P50HDM			2850-1233-6107
DESCRIPTION			PART NO.
AmTRAN TECHNOLOGY Co., LTD.	THIRD ANGLE PROJECTION	MODEL No.:	VIZIO P50HDM
UNLESS OTHERWISE NOTED .XX = ±0.10 .X = ±0.2 ANG. = ±1/2°	DSN: JESSIE Yu 07/20/'04	MATERIAL: ******	DWG. NAME: 50" CASE ASS'Y
	CHK:	QTY: 1 SIZE: A1	
		SCALE: Full UNIT: MM	DWG. No.: VIZIO-P50HDM-PLA50-AU-CA.DWG REV. 0 SHEET: 1 of 1